RIKEN QUANTUM COMPUTING

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Scaling up superconducting quantum circuits with tileable qubit architecture

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RIKEN Center for Quantum Computing

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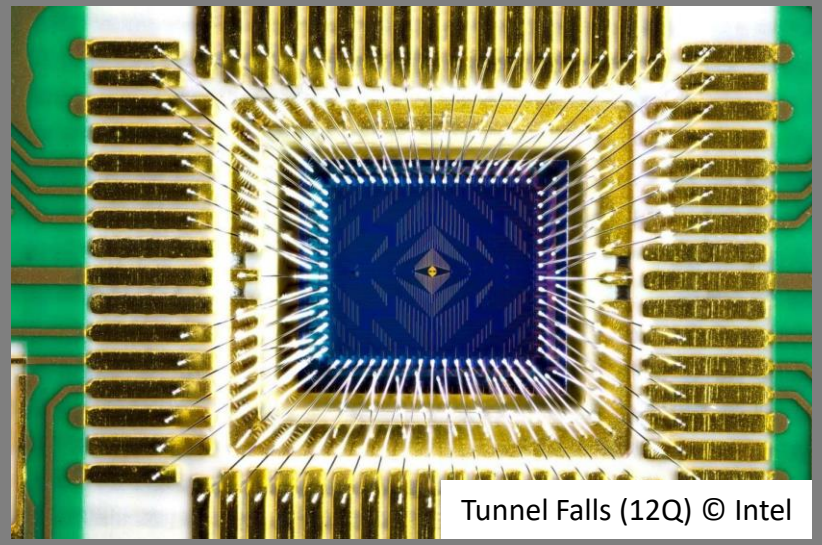
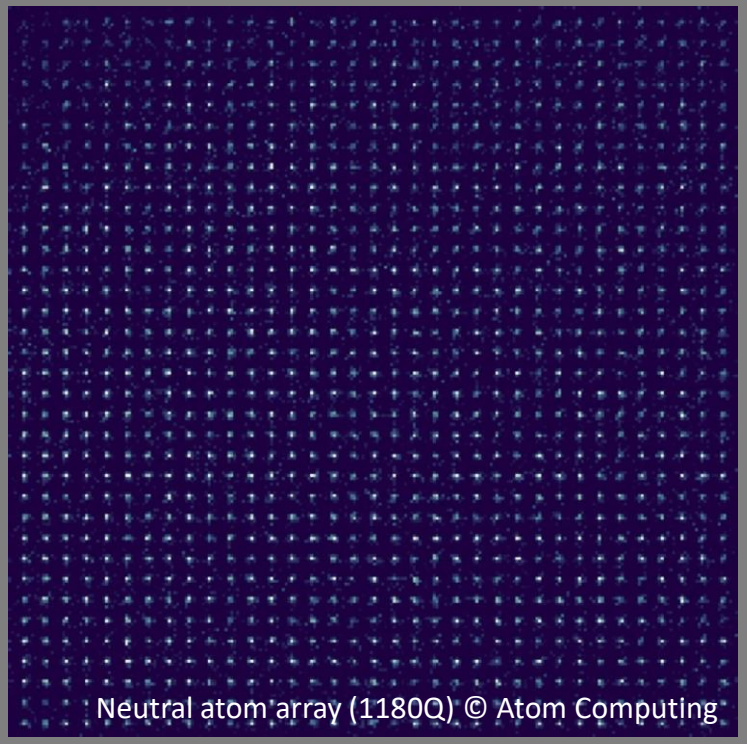
APS Global Physics Summit, Session MAR-G18.07

@Anaheim Convention Center

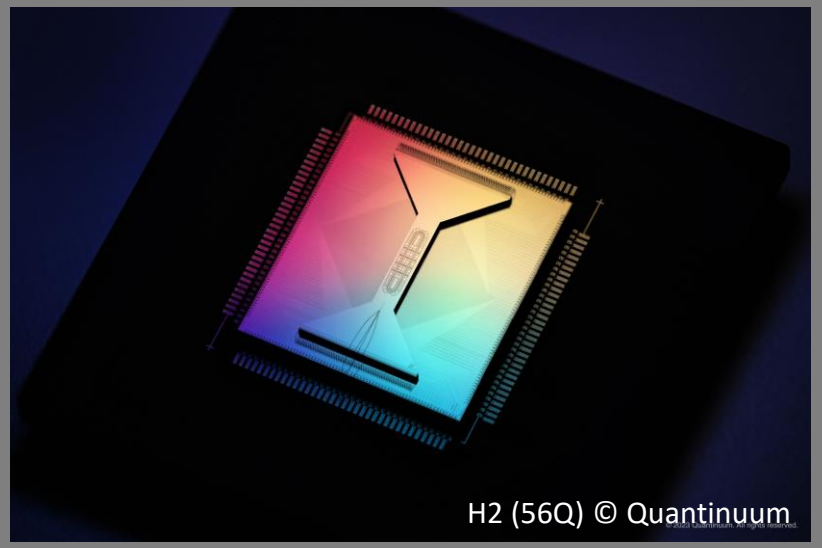
The rise of quantum computing

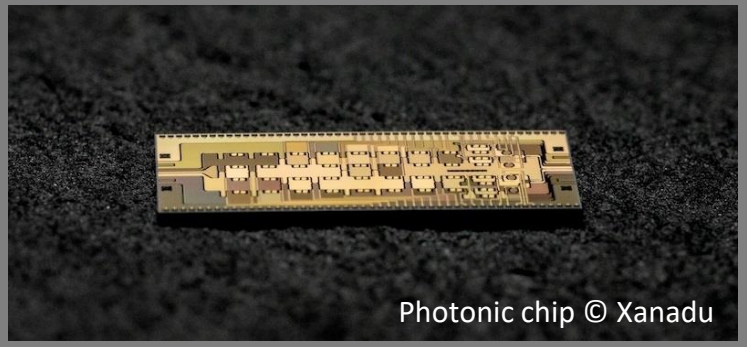

Willow (105Q) © Google


Tunnel Falls (12Q) © Intel


Neutral atom array (1180Q) © Atom Computing

Heron R2 (156Q) © IBM


H2 (56Q) © Quantinuum


Photonic chip © Xanadu

https://quantumai.google/
https://research.ibm.com/quantum-computing

https://www.intel.com/content/www/us/en/newsroom/news/quantum-computing-chip-to-advance-research.html
https://www.quantinuum.com/

https://atom-computing.com/
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Superconducting quantum computers

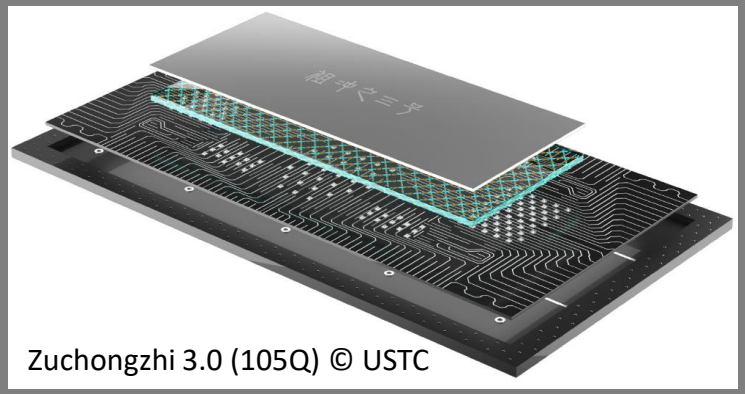
Willow (105Q) © Google

Article

Quantum error correction below the surface code threshold

https://doi.org/10.1038/s41586-024-08449-y Google Quantum AI and Collaborators*

Nature **638**, 920 (2025)
Google Quantum AI and Collborators



Zuchongzhi 3.0 (105Q) © USTC

Heron R2 (156Q) © IBM

PHYSICAL REVIEW LETTERS **134,** 090601 (2025)

Editors' Suggestion | Featured in Physics

Establishing a New Benchmark in Quantum Computational Advantage with 105-qubit Zuchongzhi 3.0 Processor

Phys. Rev. Lett. **134**, 090601 (2025) D. Gao *et al.*

Nature **618**, 500 (2023) Y. Kim *et al.*

Article

Evidence for the utility of quantum computing before fault tolerance

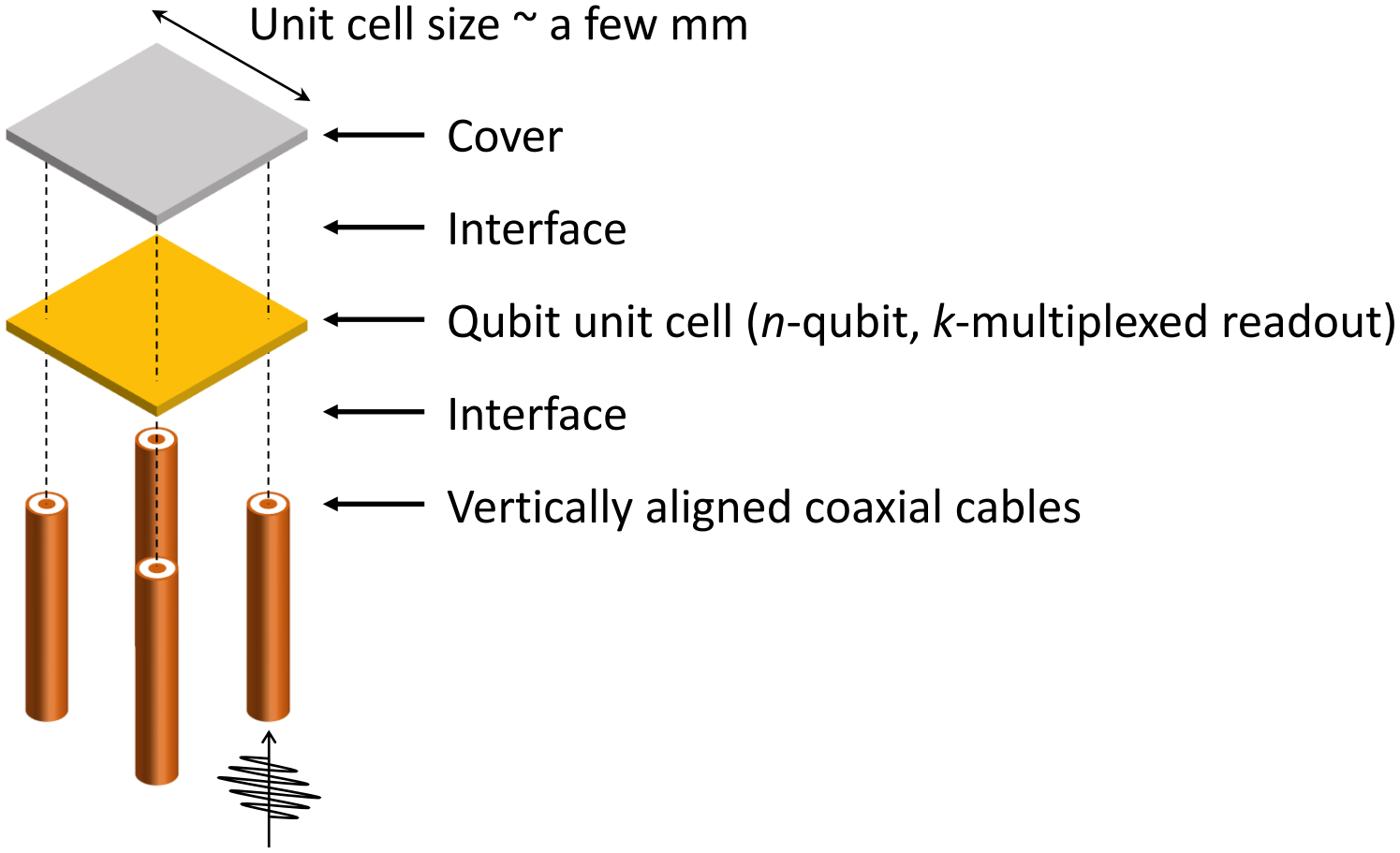
https://doi.org/10.1038/s41586-023-06096-3
Received: 24 February 2023

Youngseok Kim[1,6], Andrew Eddins[2,6], Sajant Anand[3], Ken Xuan Wei[1], Ewout van den Berg[1], Sami Rosenblatt[1], Hasan Nayfeh[1], Yantao Wu[3,4], Michael Zaletel[3,5], Kristan Temme[1] & Abhinav Kandala[1]

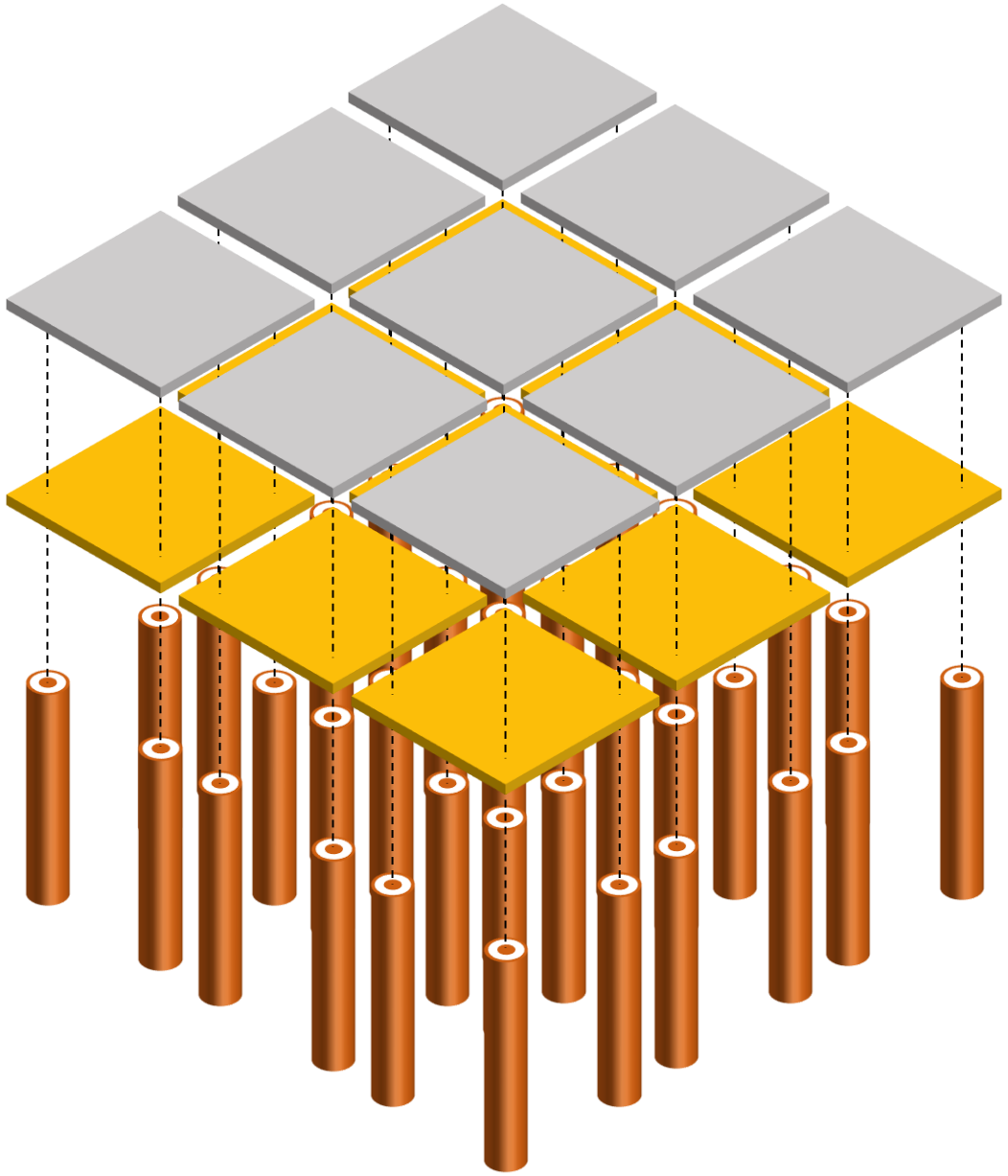
Many companies and academic research groups around the world

https://quantumai.google/
https://research.ibm.com/quantum-computing

Tileable architecture including wiring



Tileable architecture including wiring



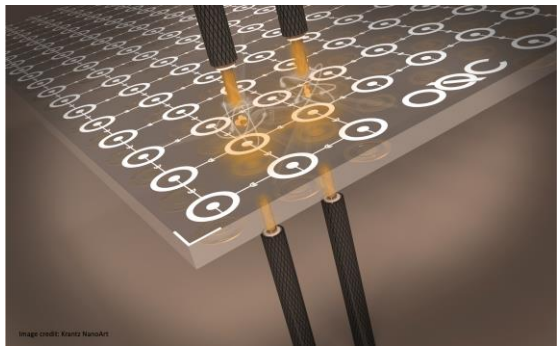
Cover chip

Indium bump

Chip consisting of tiled **4-qubit, 4-mux RO unit cells**

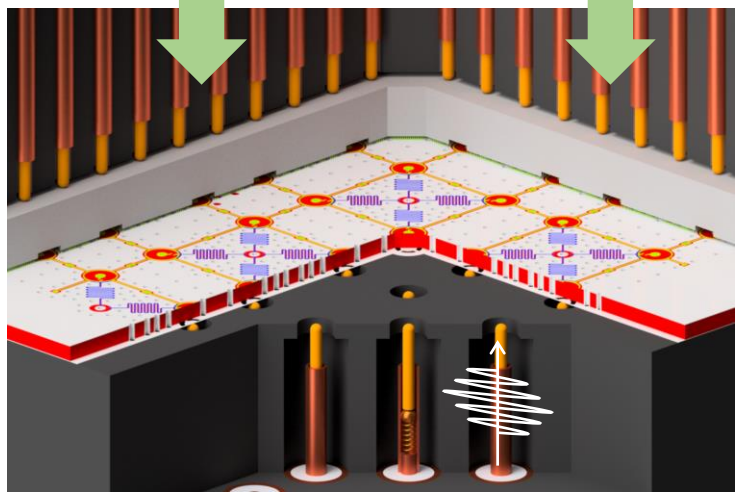
Pogo-pin package

1.19-mm coaxial cables

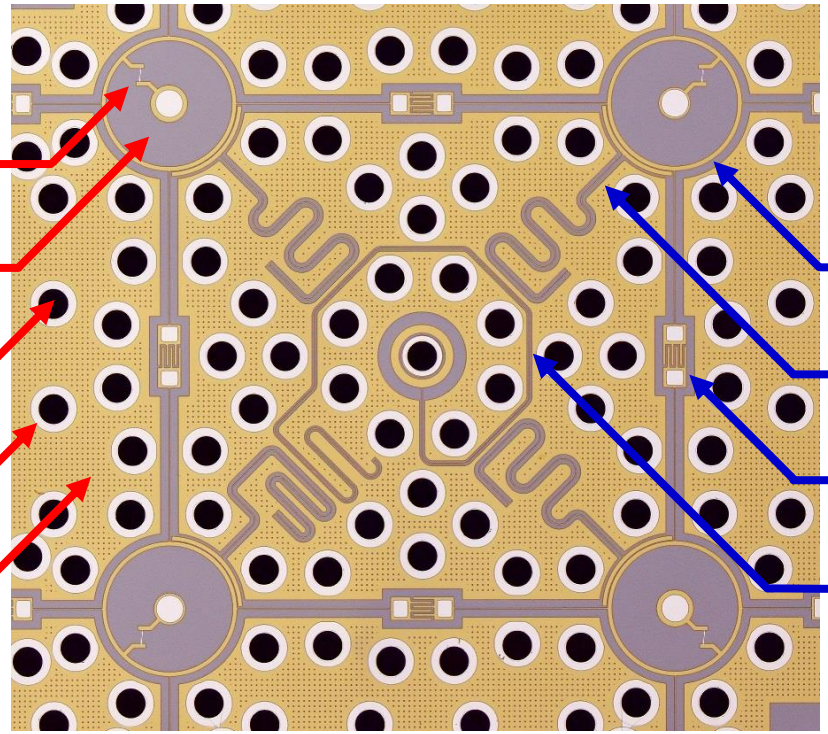


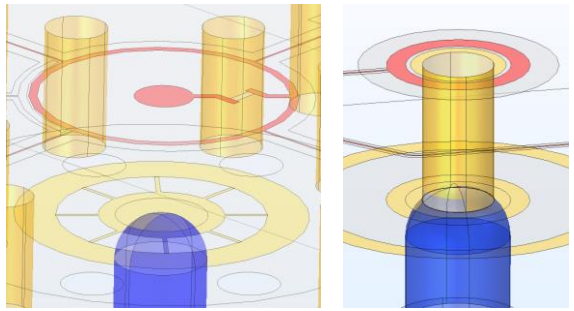
Coaxmon © OQC

Press down the chip



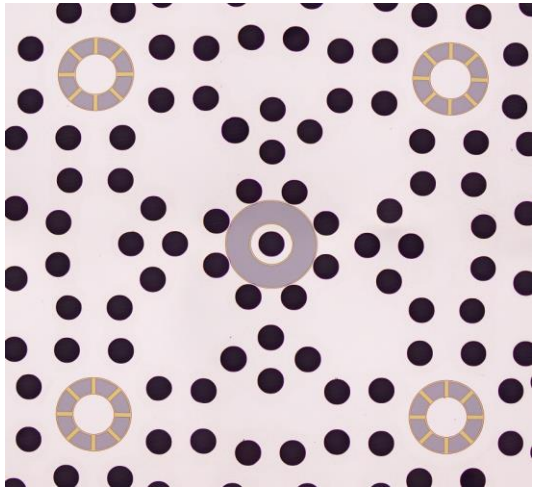
Qubit unit cell



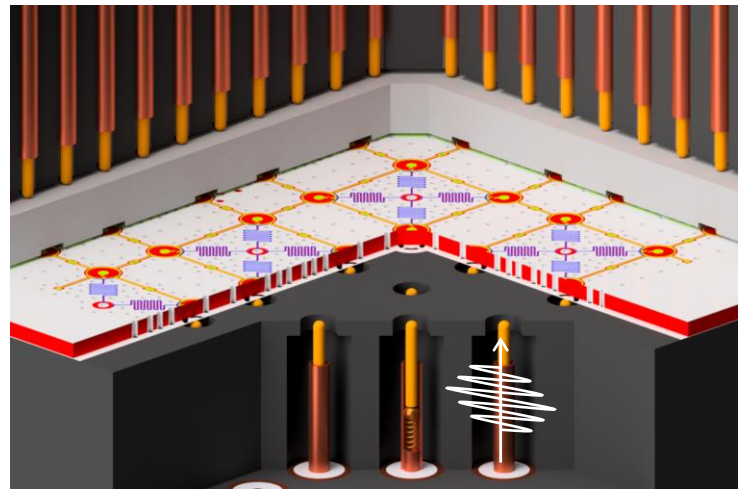


Design parameters

- f_q = 7.9–9.1 GHz (**fixed**), κ_q = 0.2 kHz
- α = −400 MHz
- f_r = 10.2–10.6 GHz, κ_r = 10 MHz
- g_{qr} = 140 MHz
- g_{qq} = 10 MHz



(Backside)



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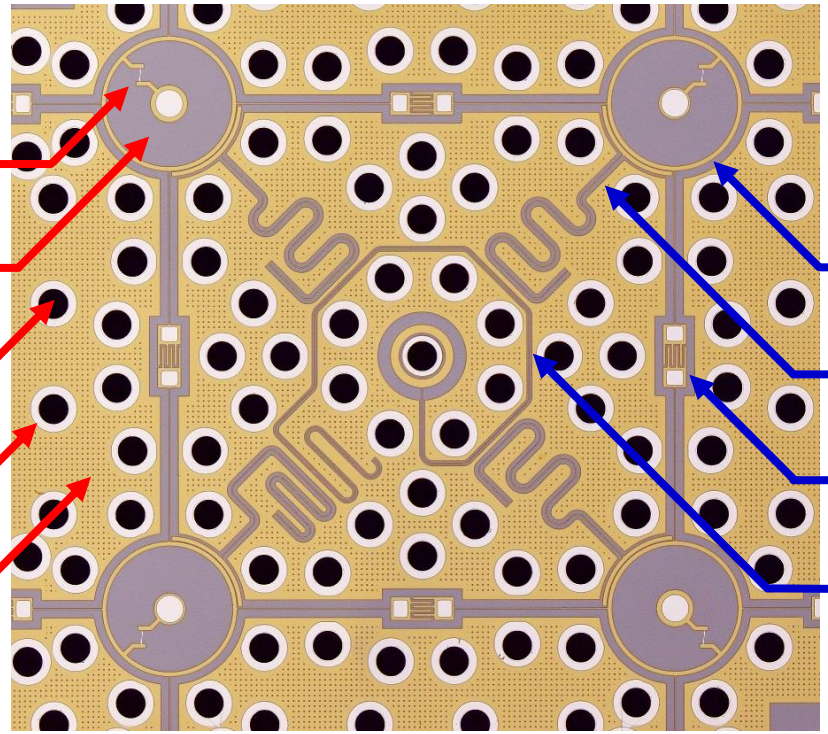

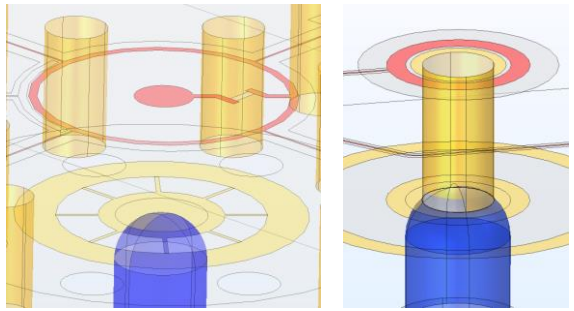

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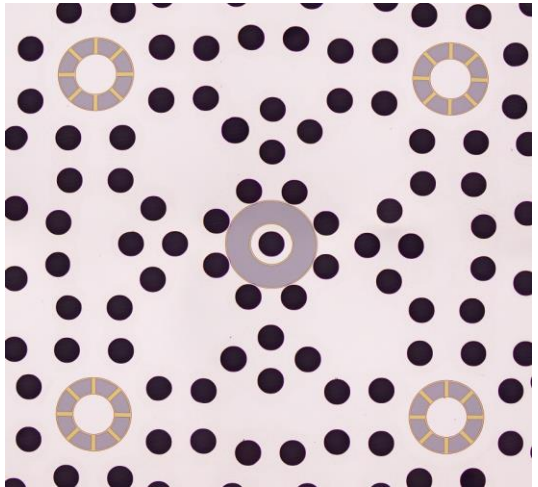

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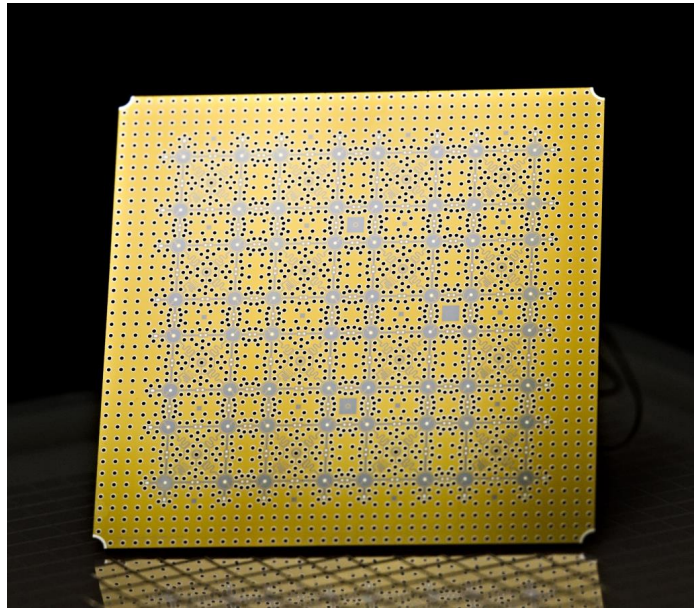
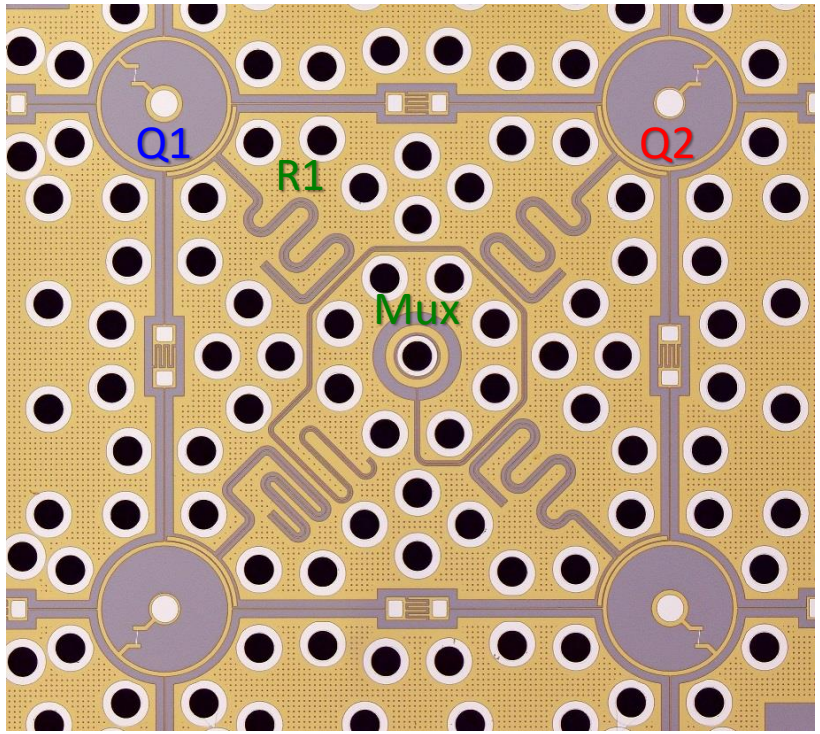
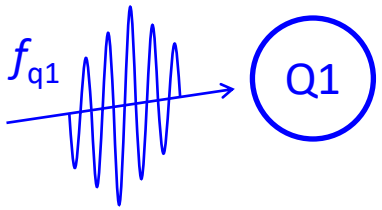


Quantum control based on circuit QED



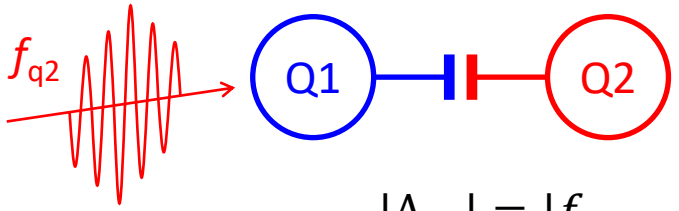
1Q gate (Rabi drive)



Microwave-only control

- **1Q & 2Q gates**
- **Readout**

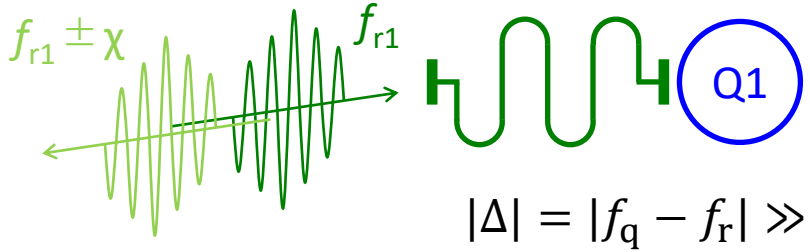
2Q gate (cross-resonance)



$\sigma_z^1 \sigma_x^2$

$$|\Delta_{12}| = |f_{q1} - f_{q2}| \gg g_{qq}$$

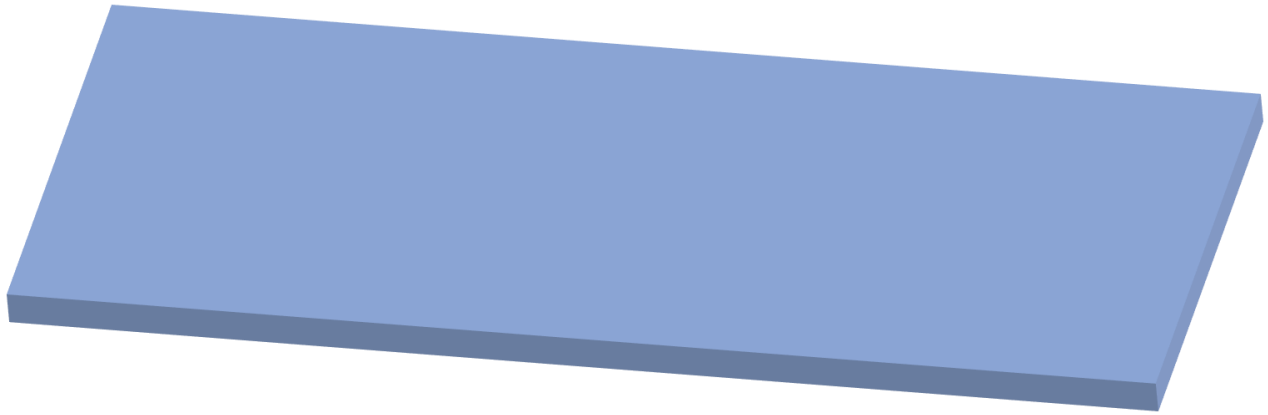
Readout (dispersive shift)



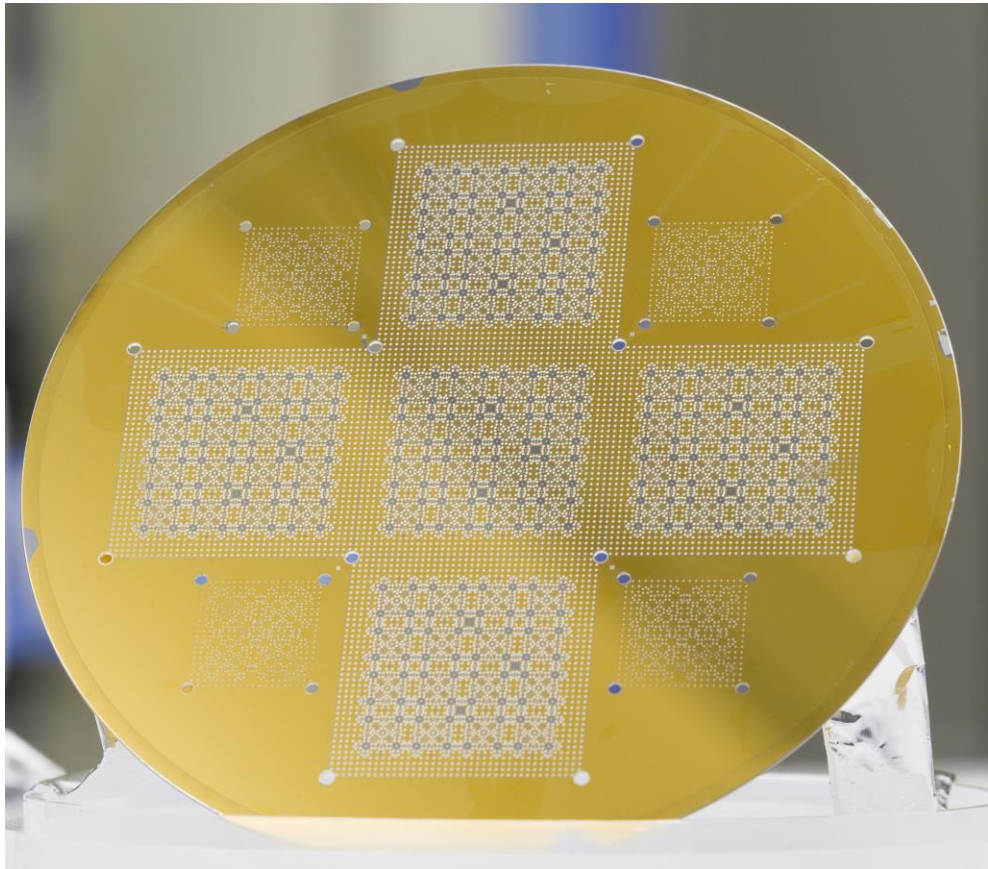
$$|\Delta| = |f_q - f_r| \gg g_{qr}, \kappa_r$$

Device fabrication

- TSV by dry etching
- TiN deposition (100 nm on both sides)
- Al deposition (300 nm on both sides, covering sidewalls with Al)
- Al structure by wet etching
- TiN structure by dry etching
- Josephson junction by shadow evaporation



3-inch, 300-µm-thick, high-resistivity wafer



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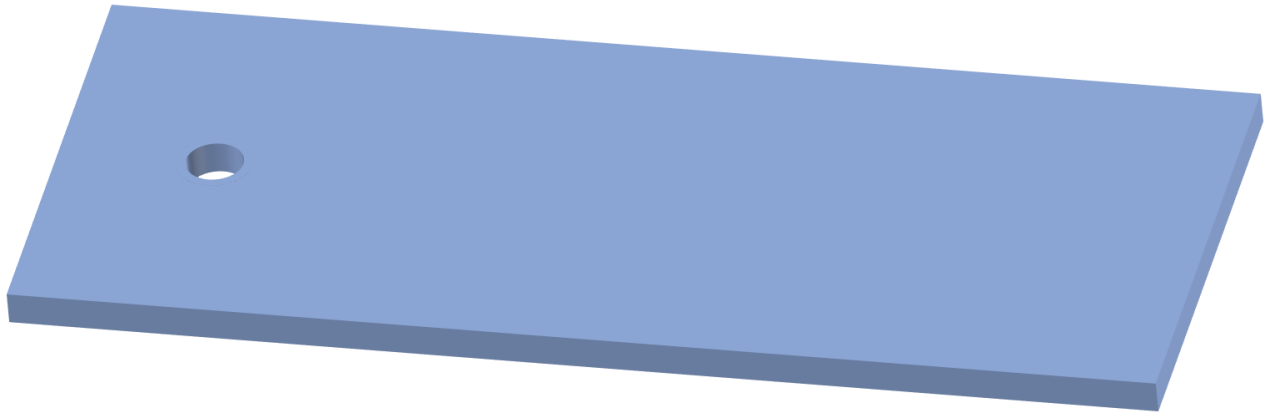
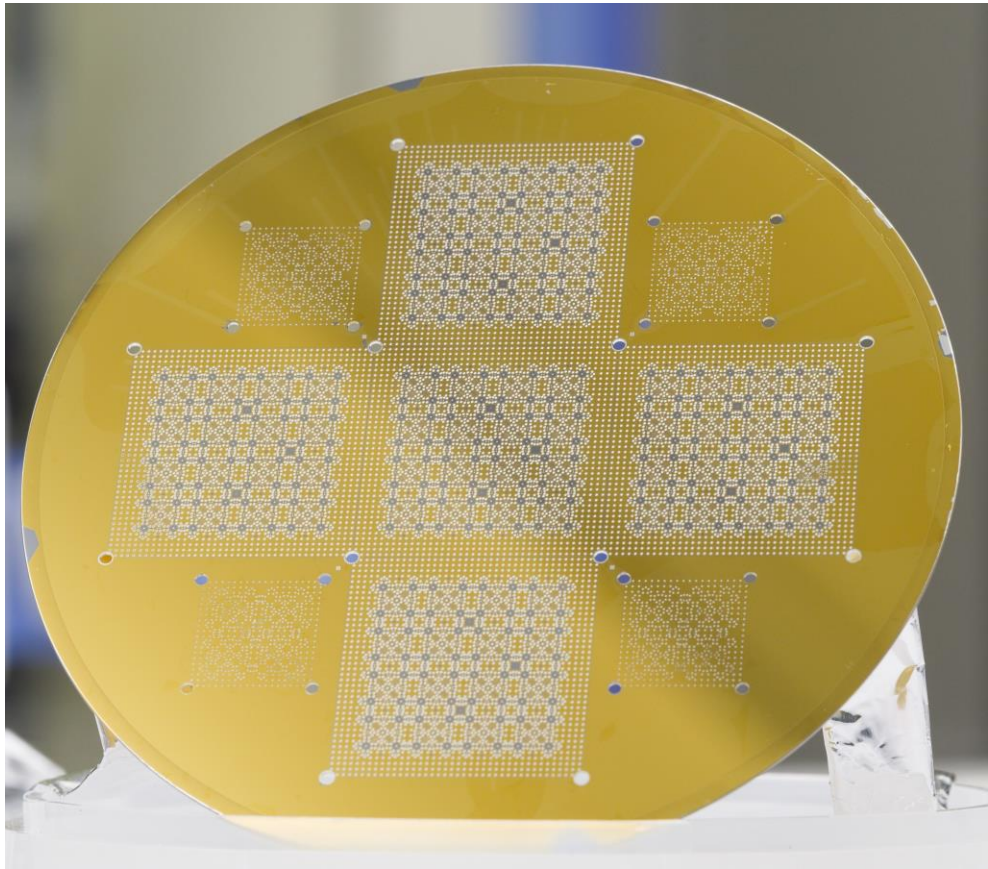


Currently, TSVs for integrated chips are outsourced



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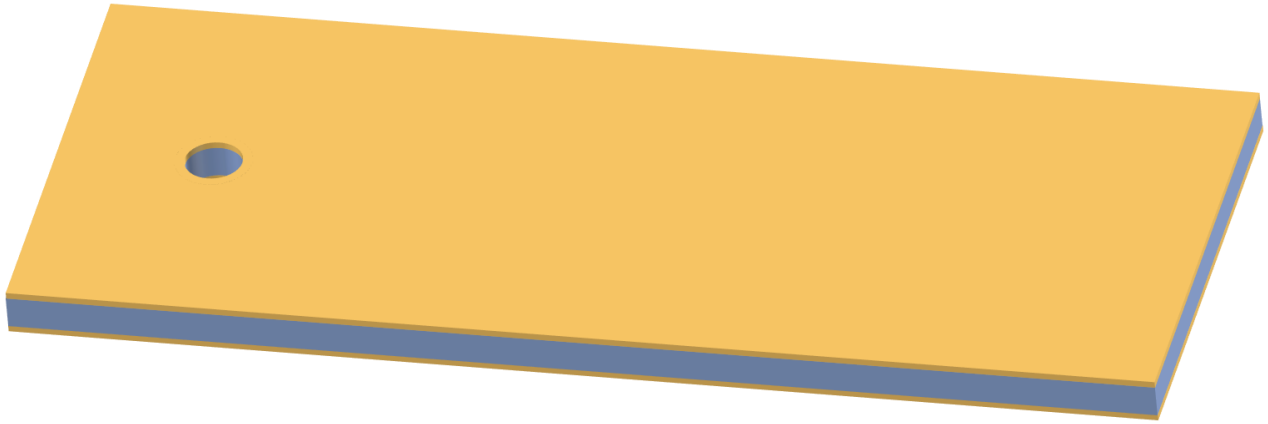
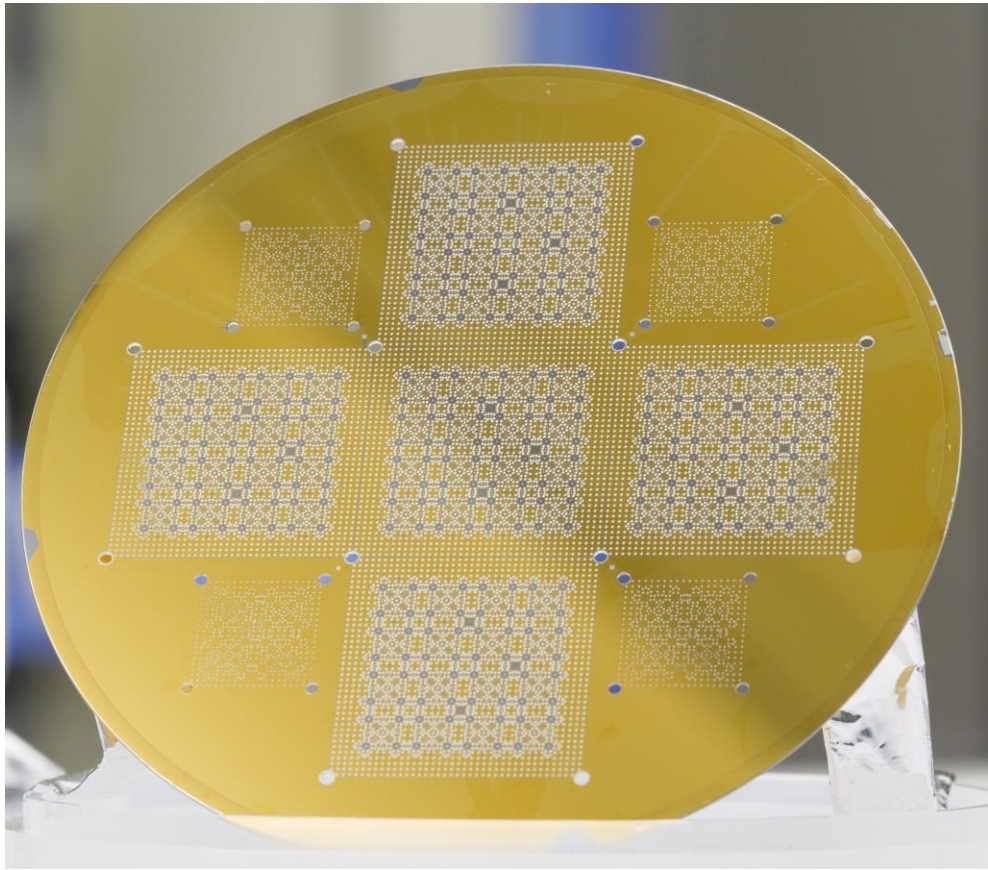


Provided by NICT (Drs. Terai and Hishida)



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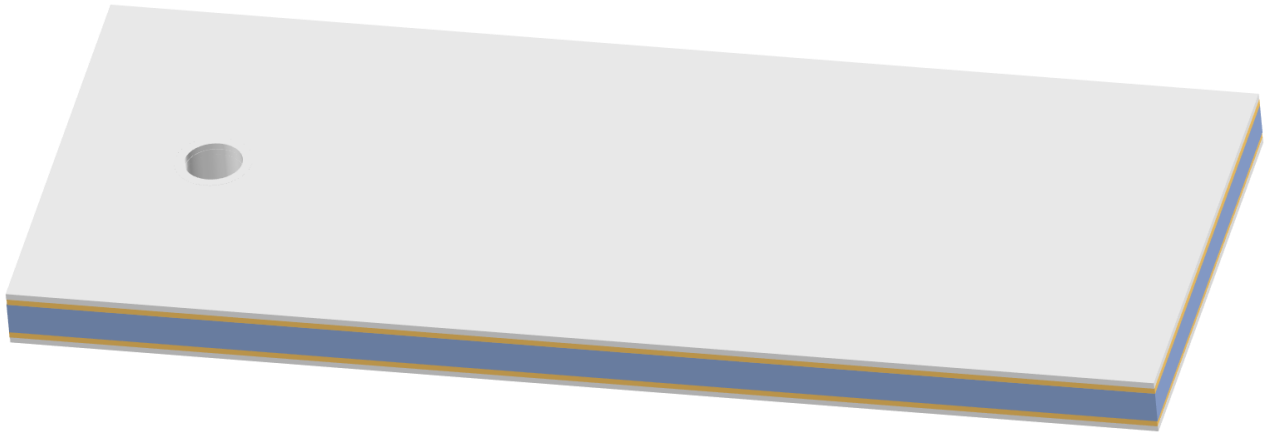
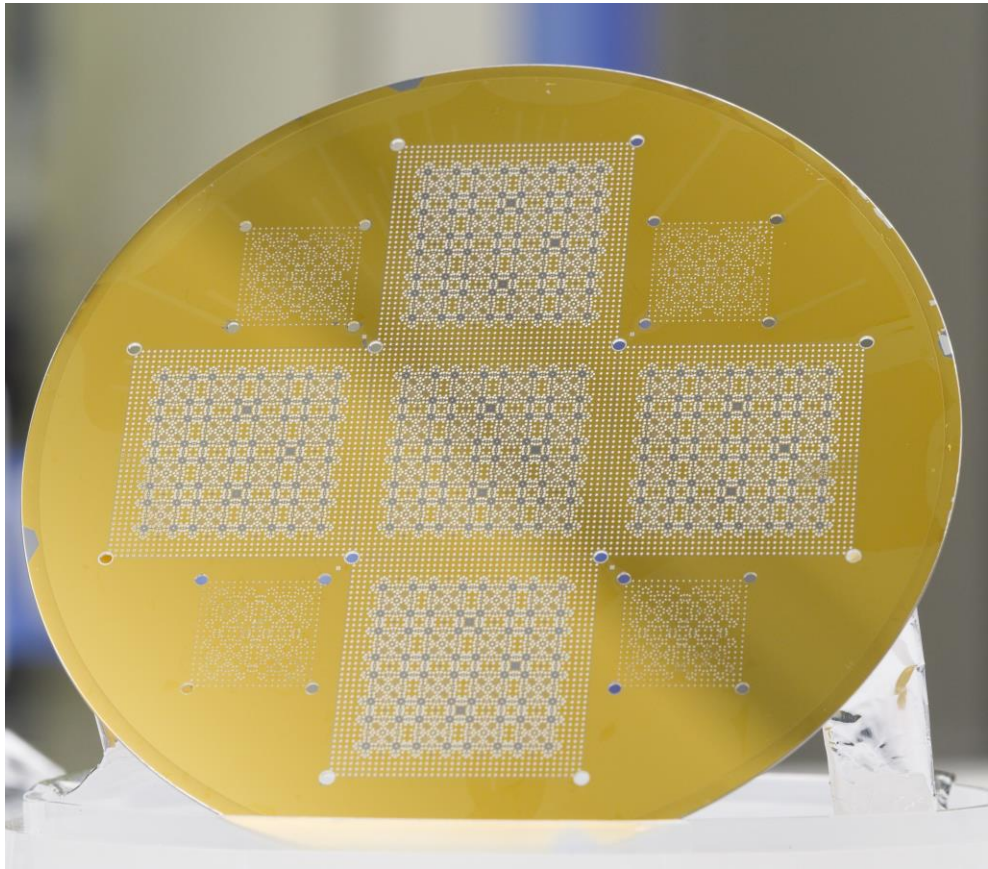


45-deg oblique deposition & rotation of the wafer



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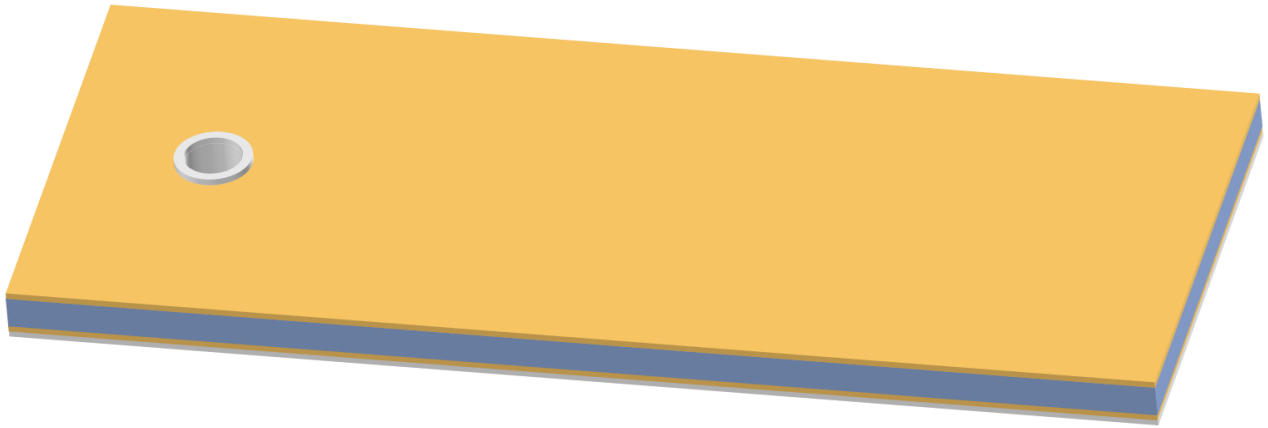
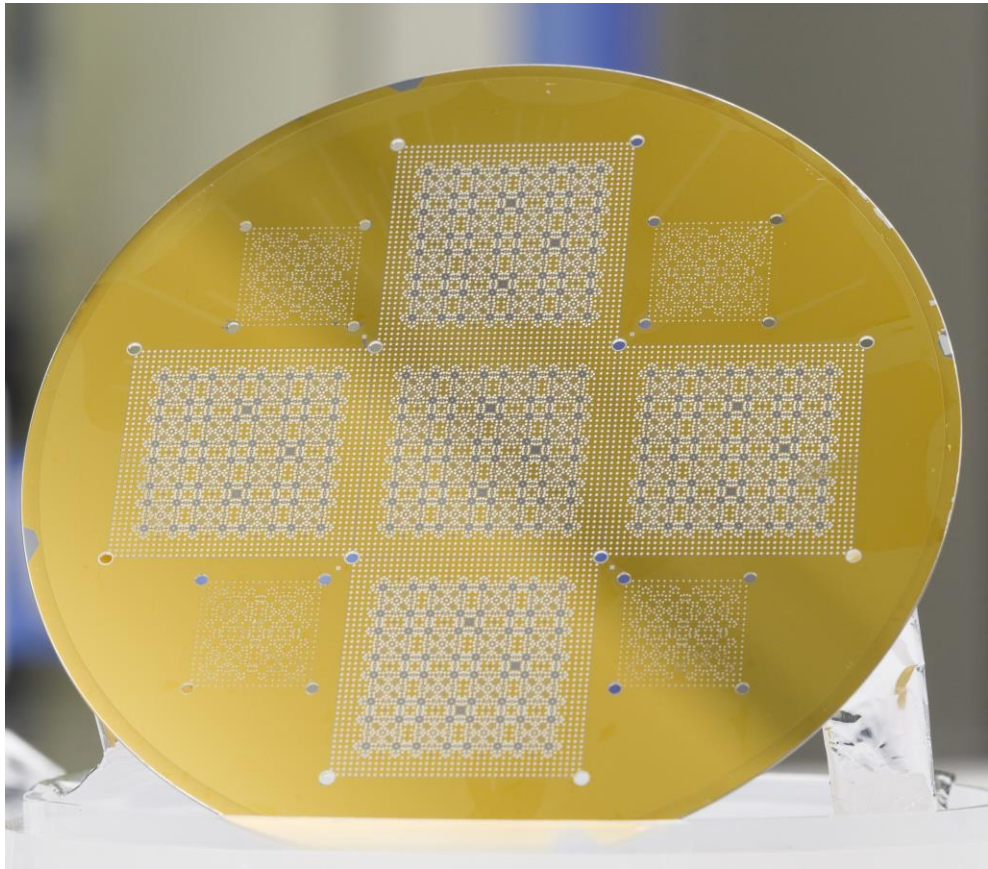


Repeat the process for the backside



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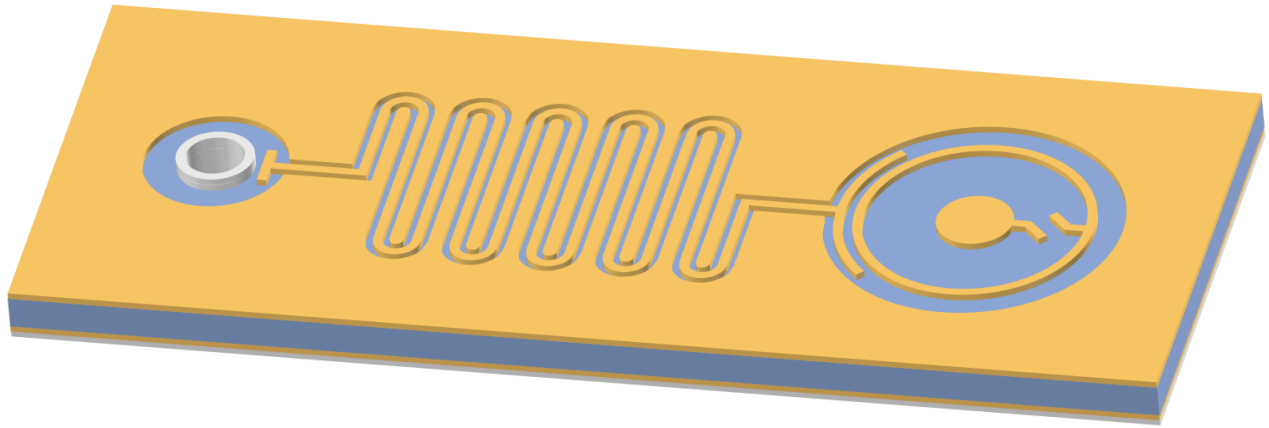

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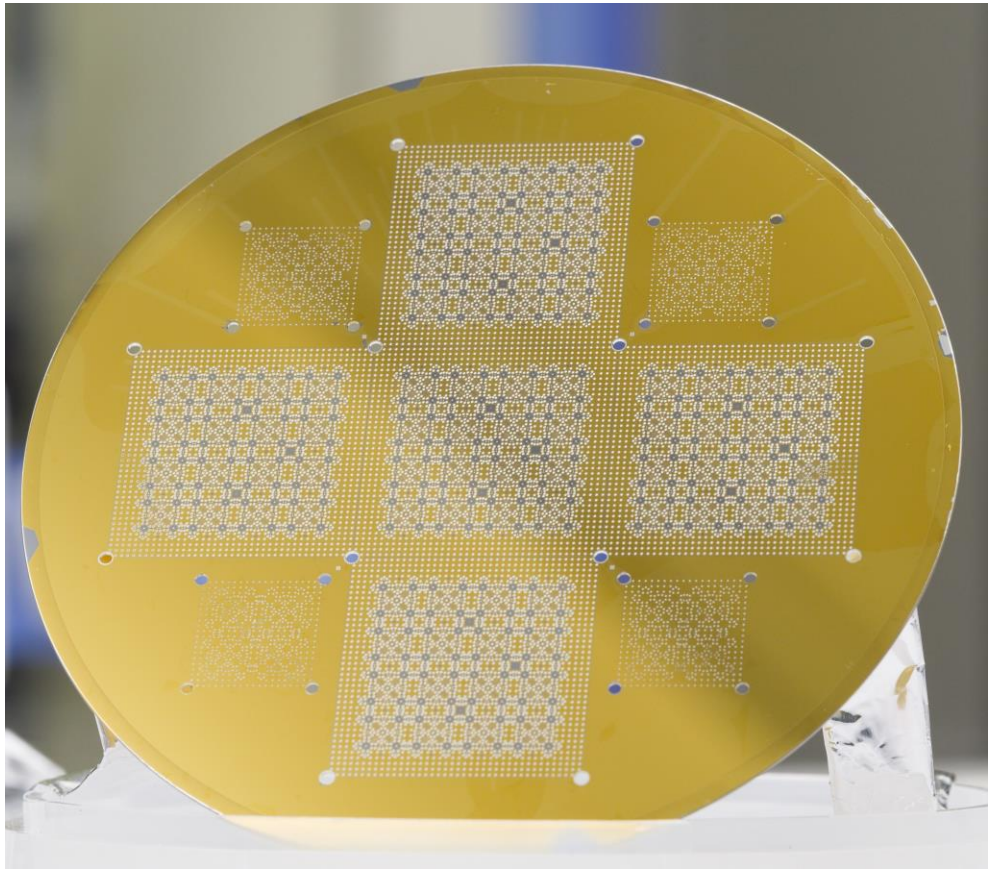

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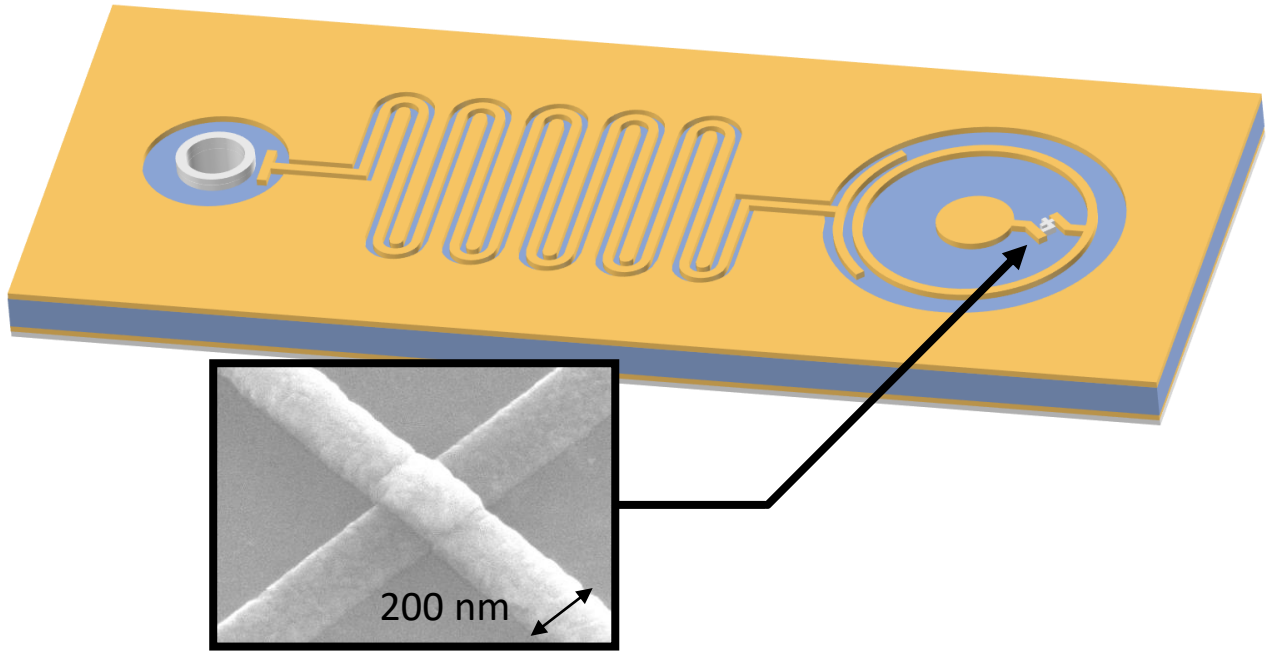

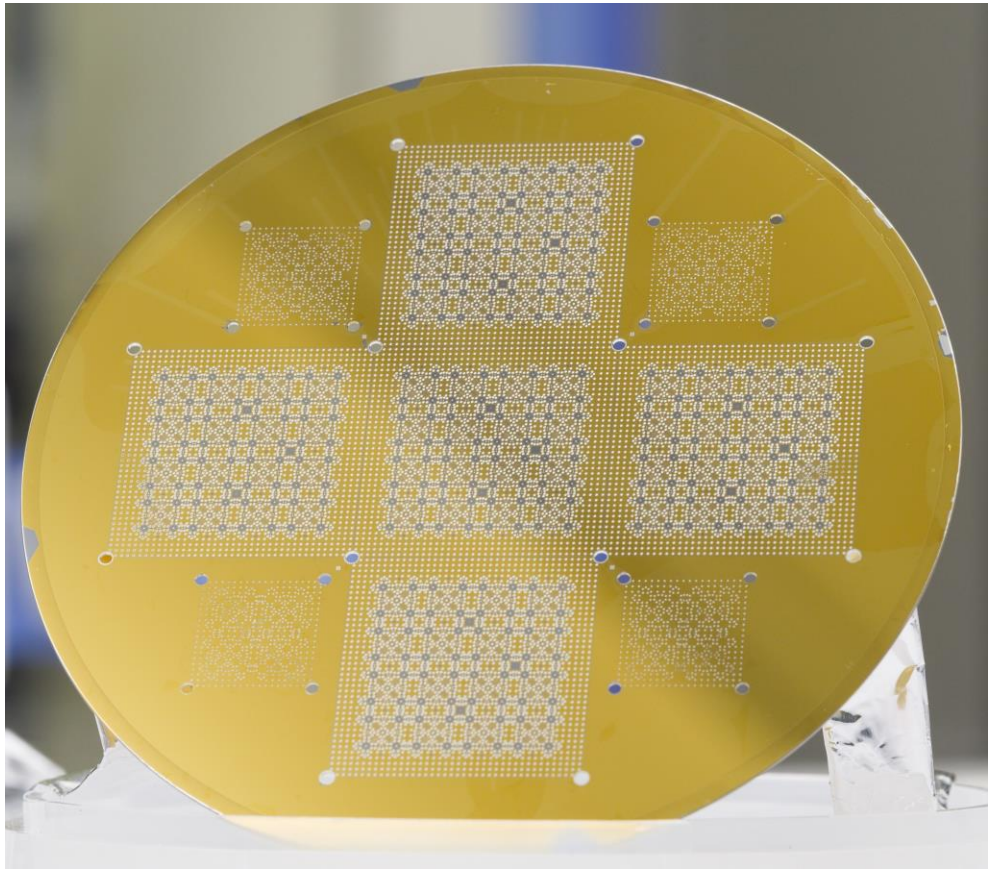

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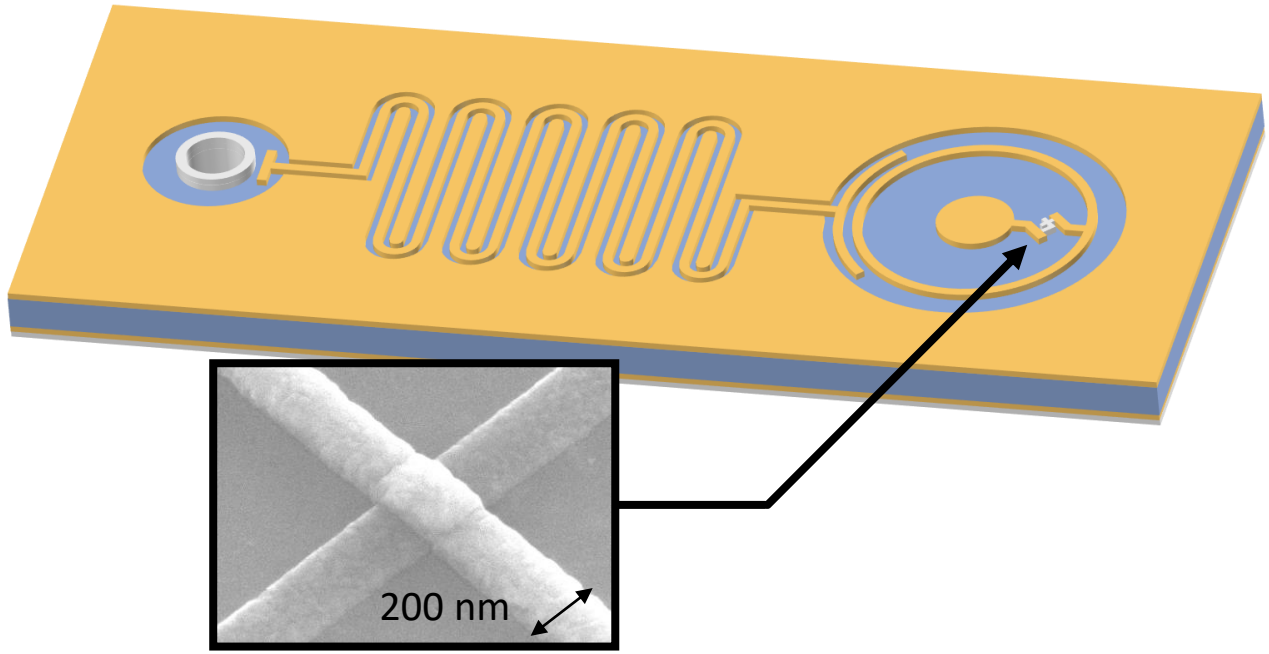
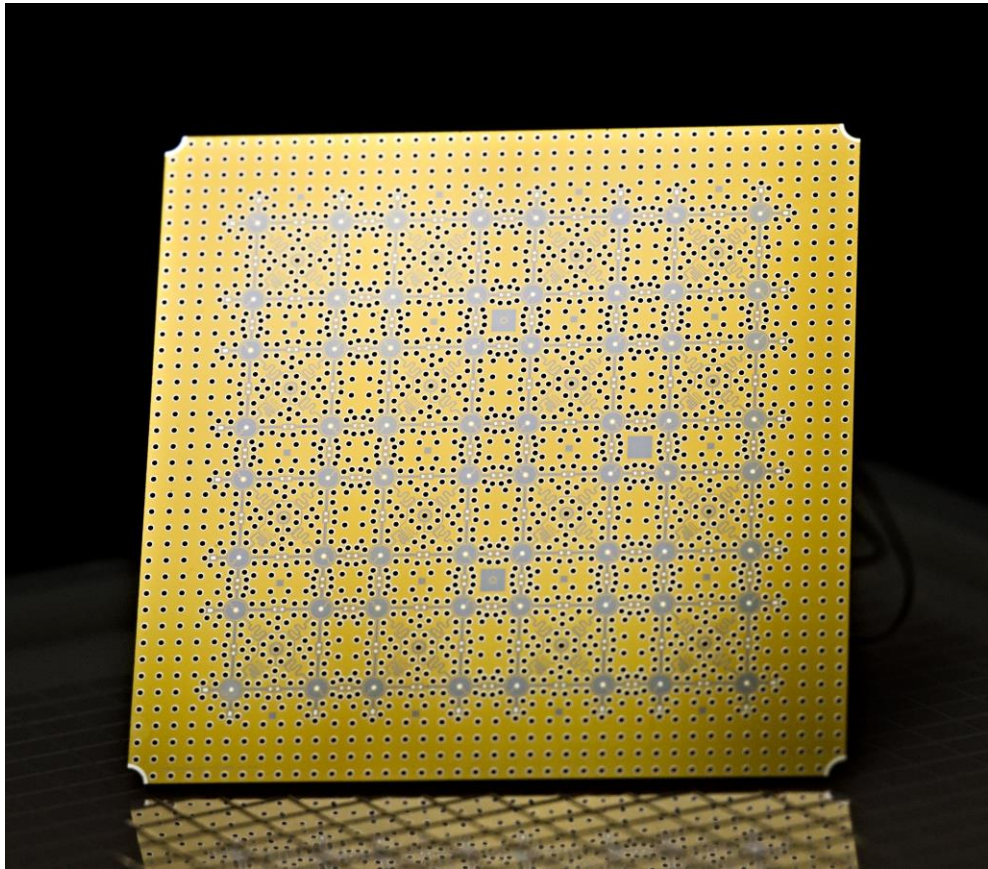




64Q system: 叡 “A”

Microwave powers & noise level

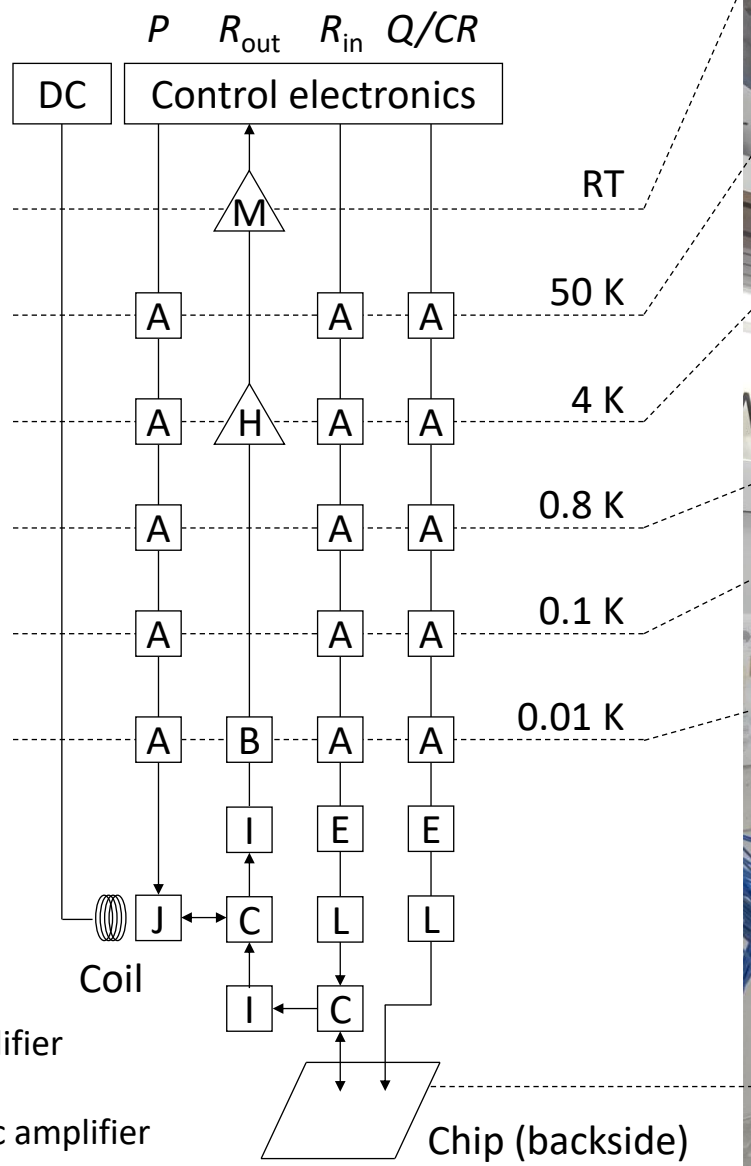
- $P_Q \approx -70$ dBm
- $P_{CR} \approx -60$ dBm
- $P_R \approx -130$ dBm
- Noise ≈ -230 dBm/Hz

# of coaxial lines for *N* qubits

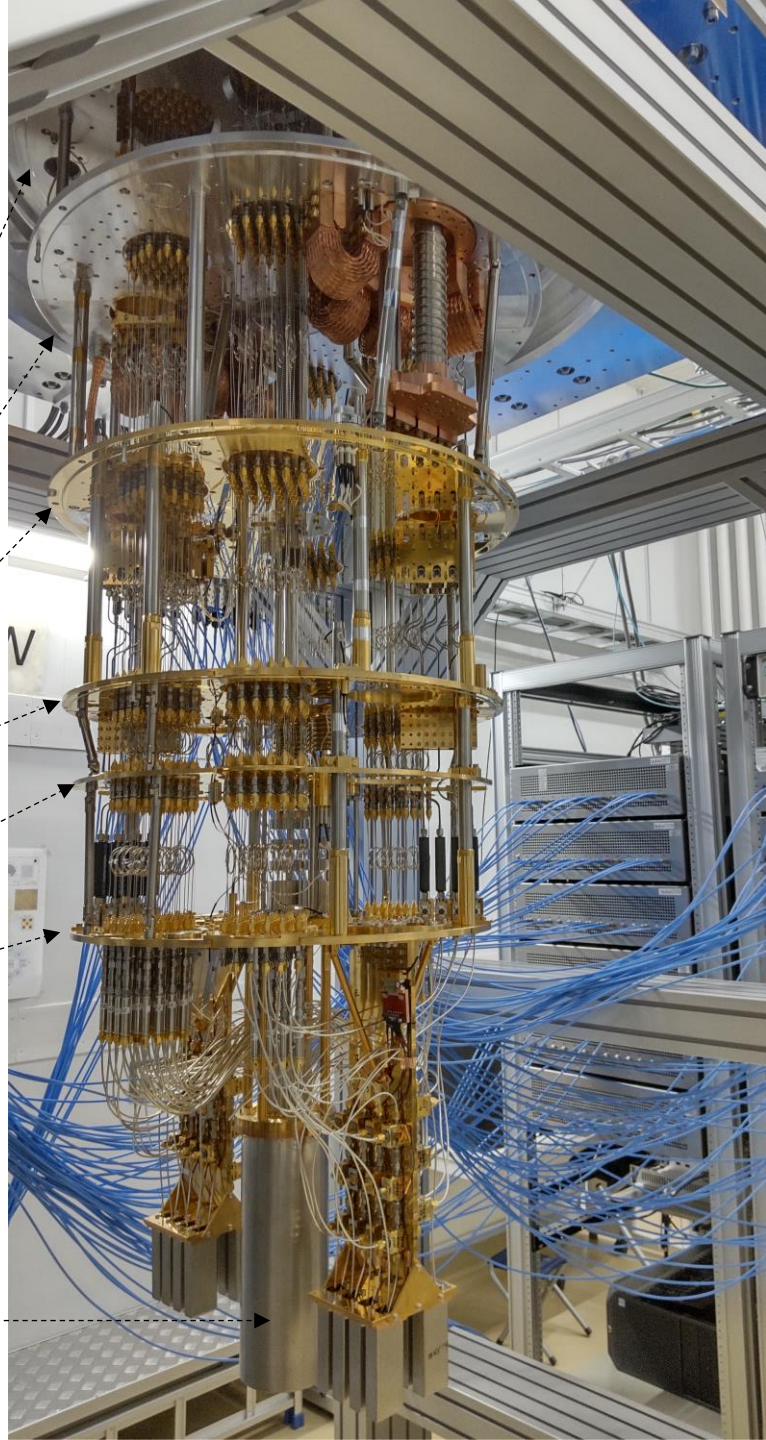
- Input: 1.25*N* to chip, 0.25*N* to JPA
- Output: 0.25*N*

Need for 64Q

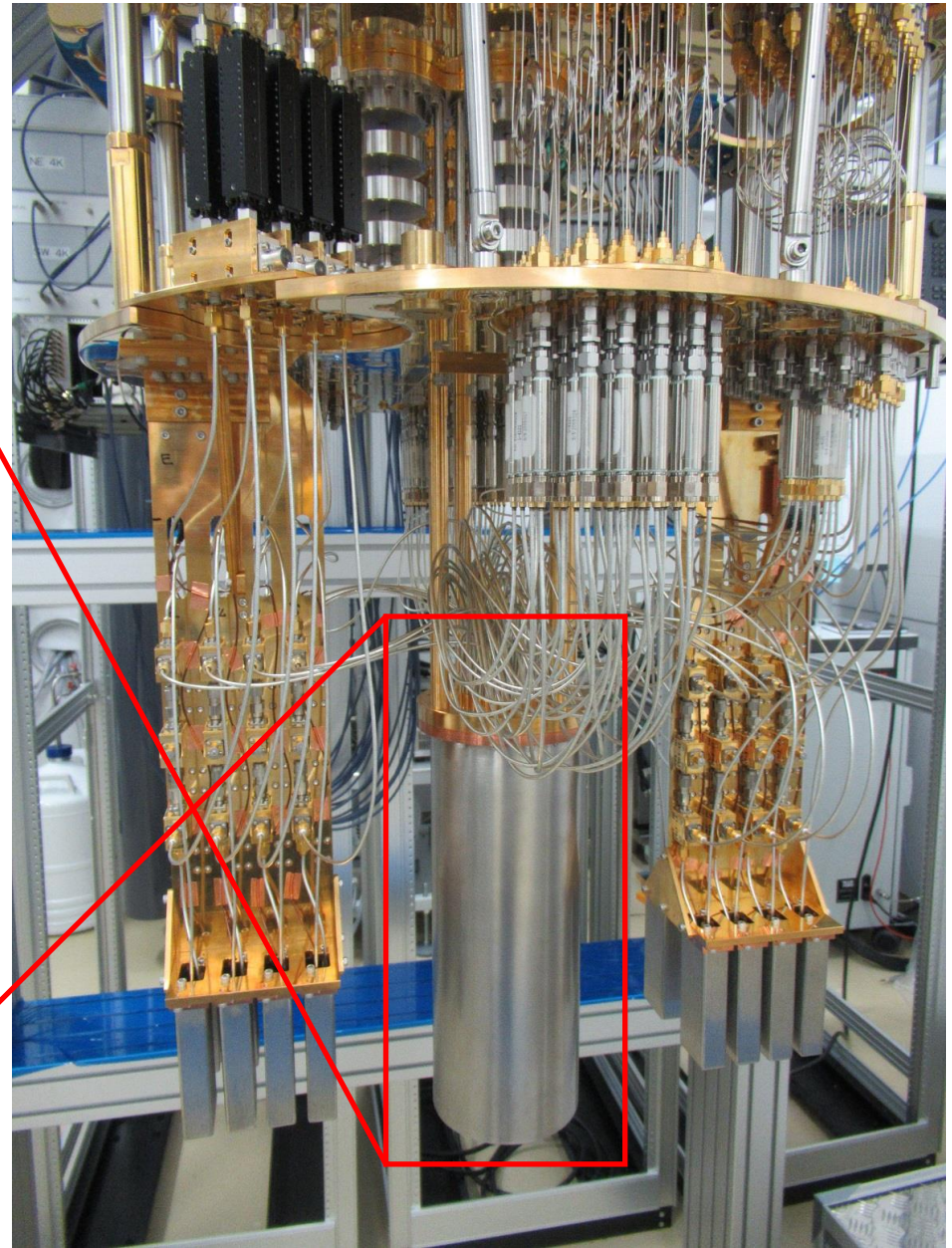
- 96 input lines
  - 64 for control
  - 16 for readout
  - 16 for JPAs
- 16 output lines
- 16 DC lines for JPAs

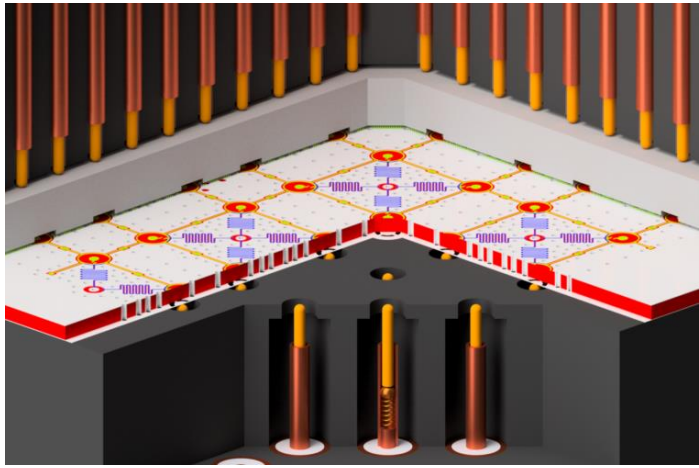


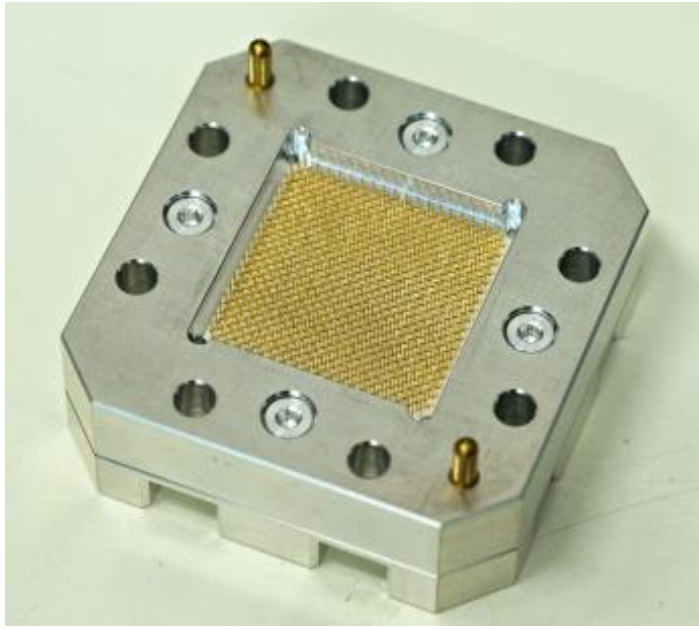
Attenuator
Eccosorb IR filter
Lowpass filter
Circulator
Isolator
Band-pass filter
HEMT cryogenic amplifier
Microwave amplifier
Josephson parametric amplifier



Sample package







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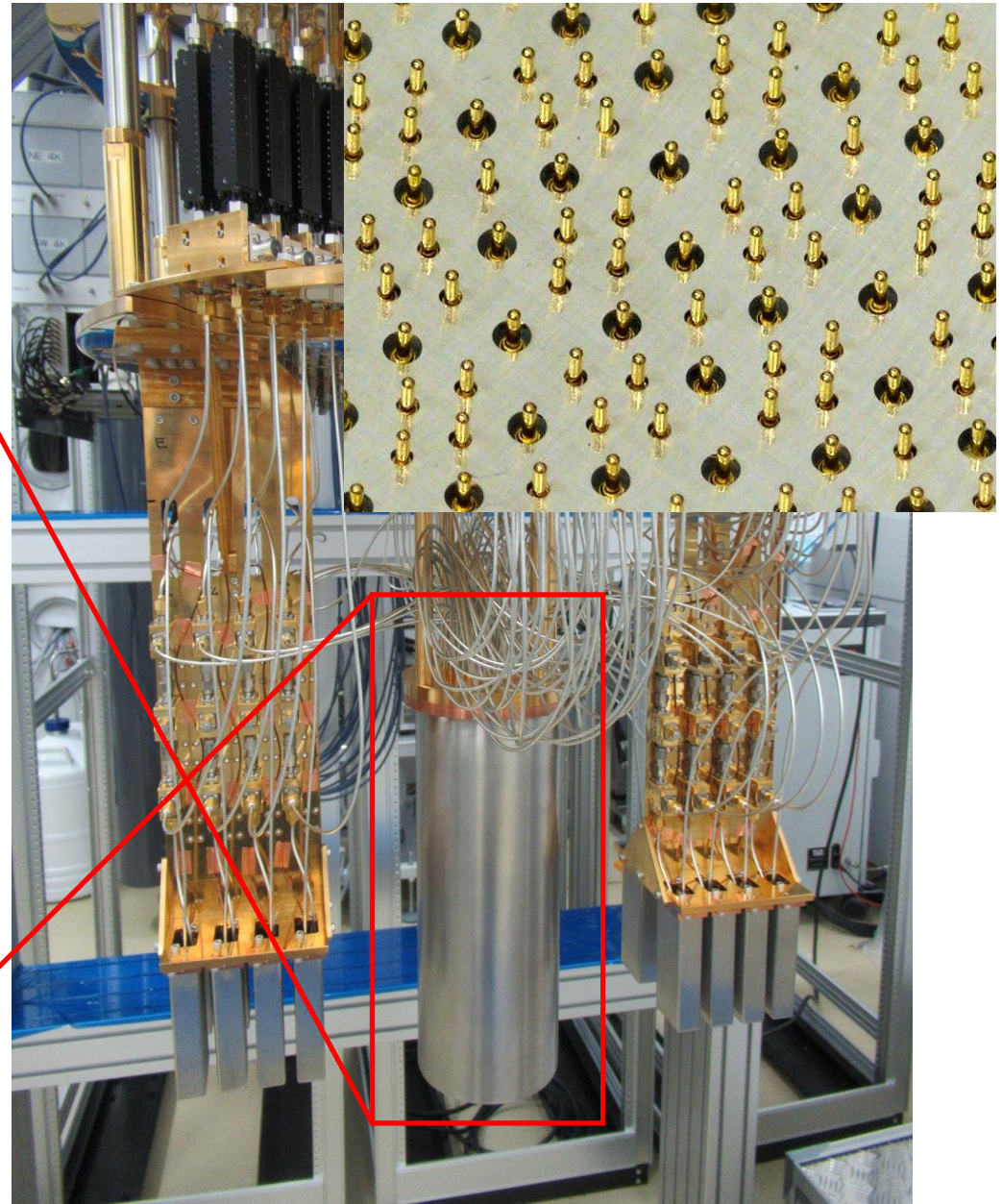

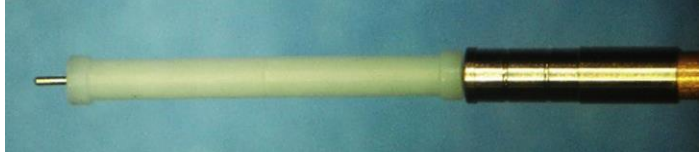

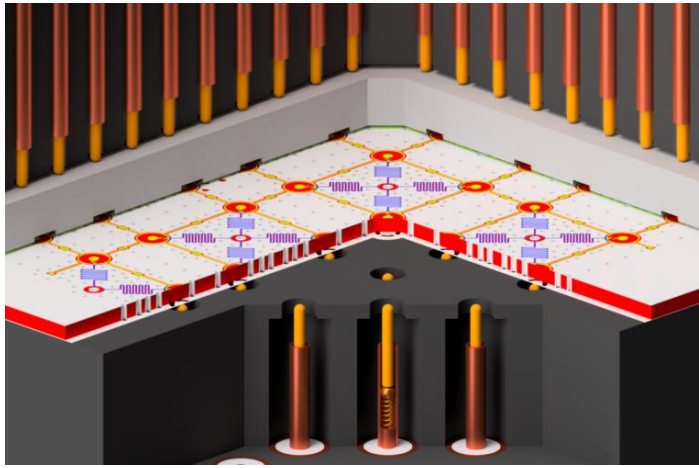

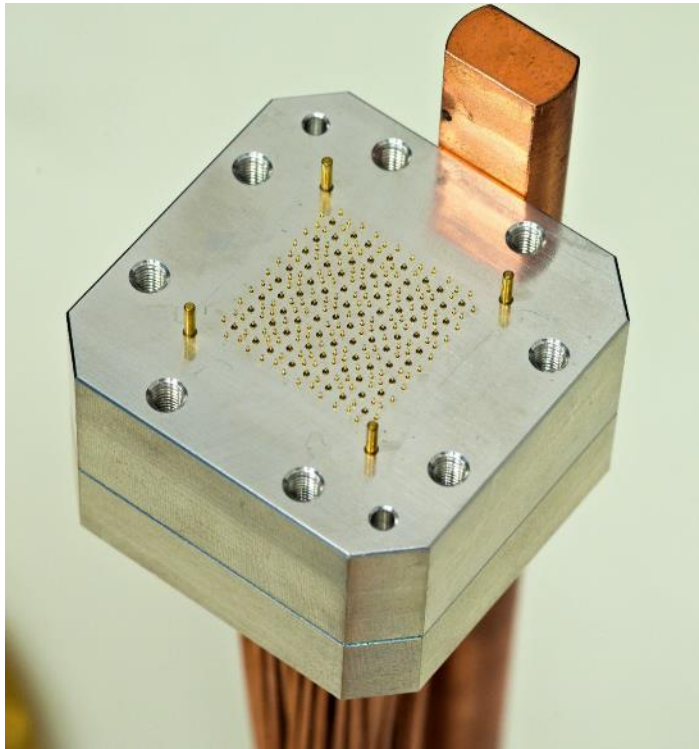

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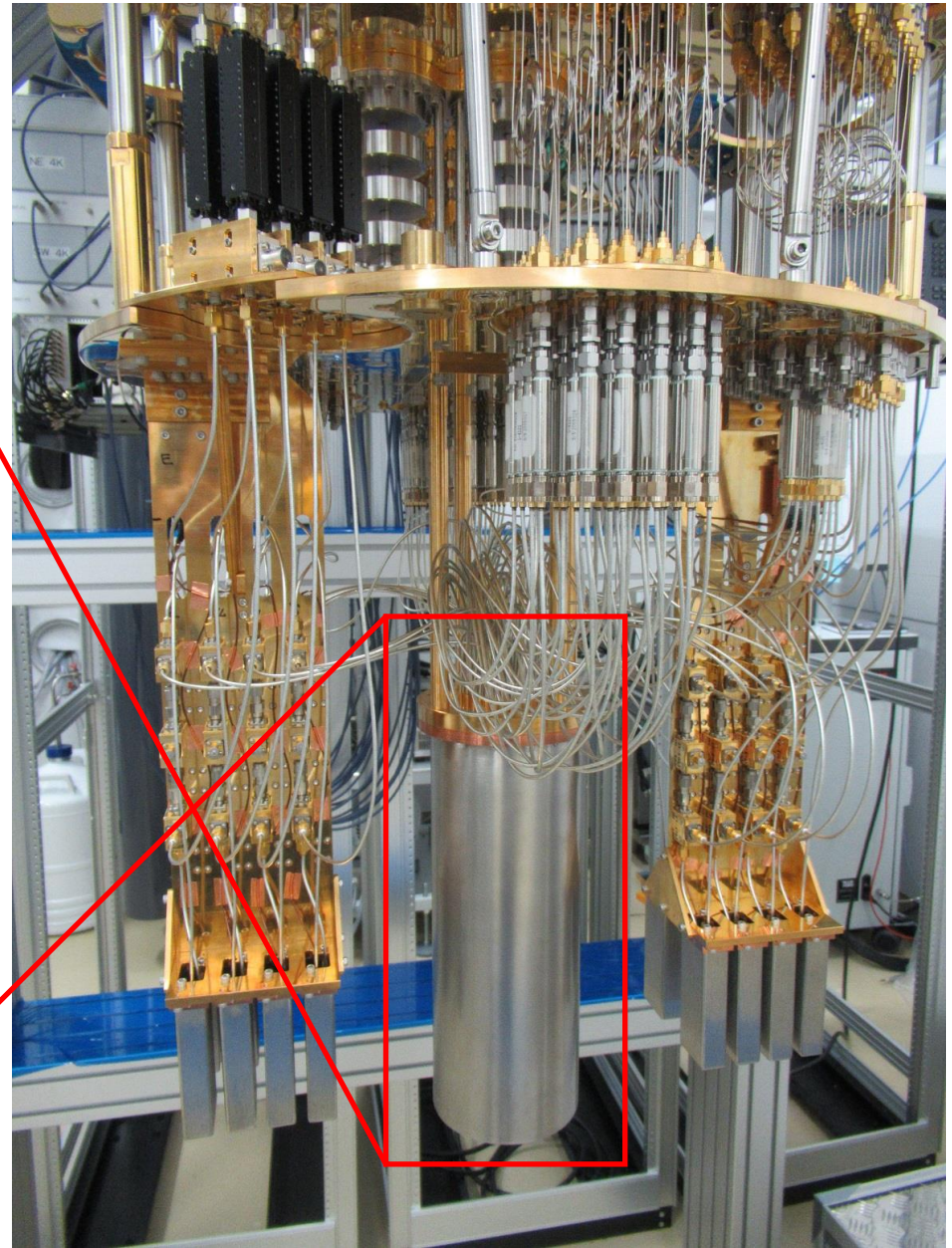
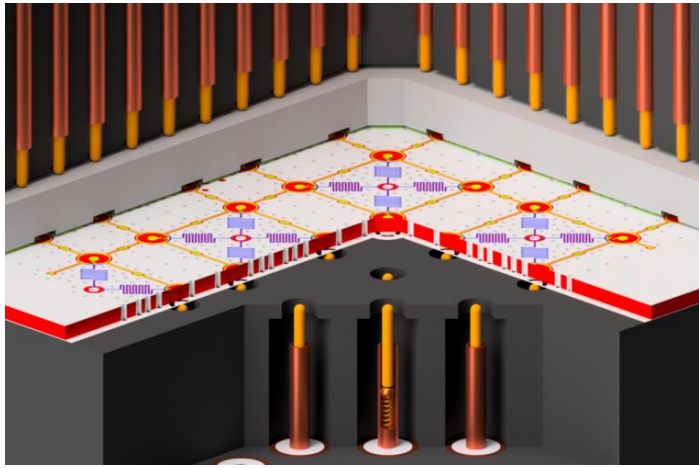
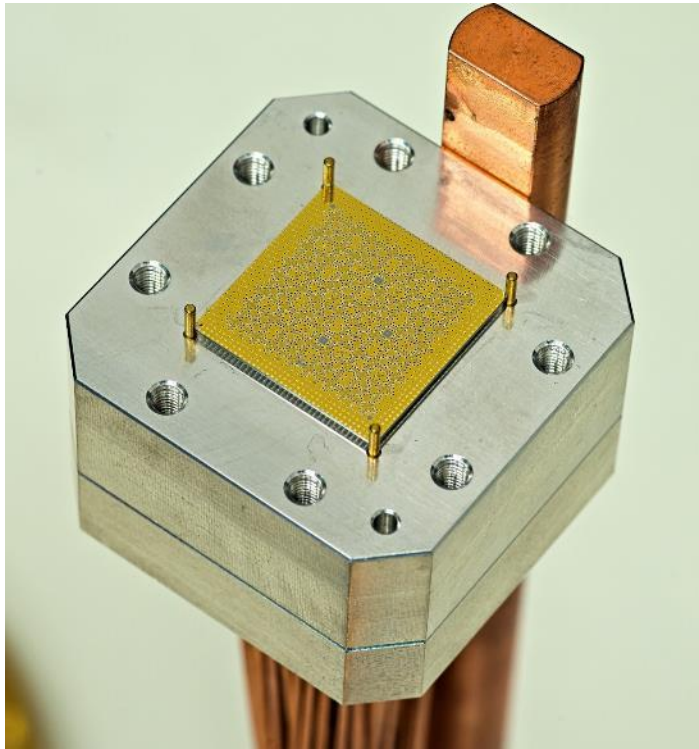
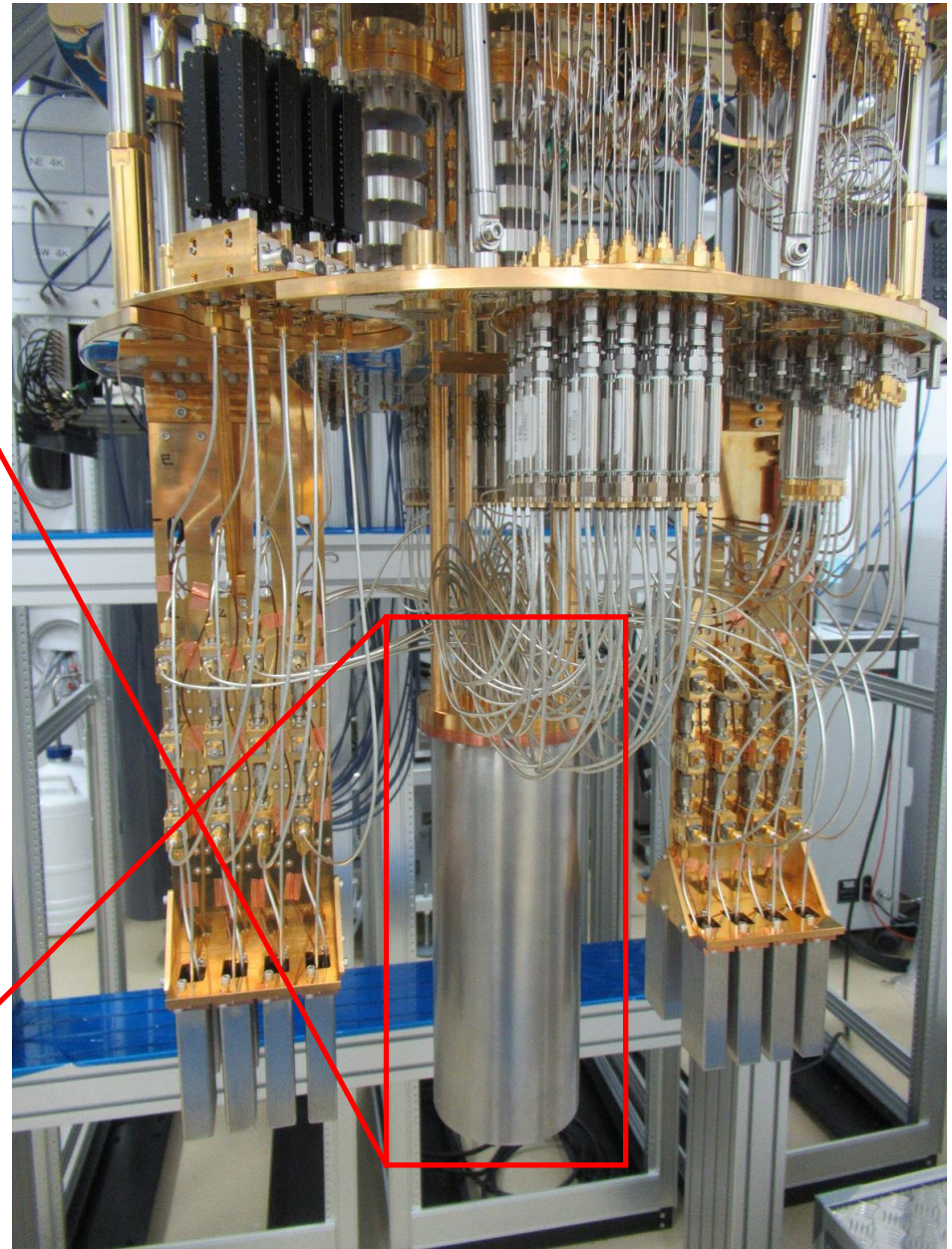
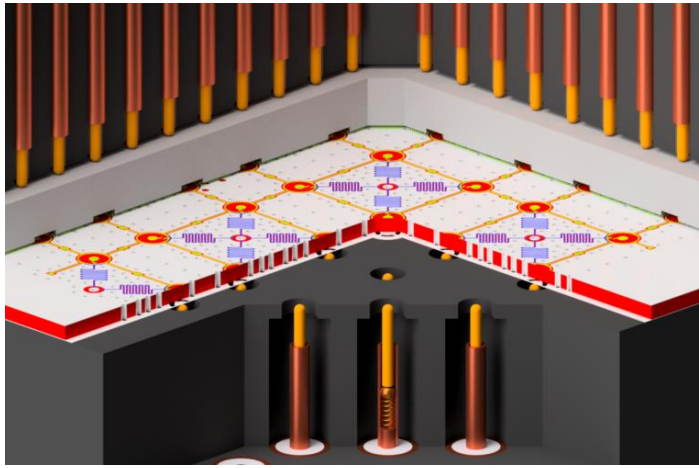


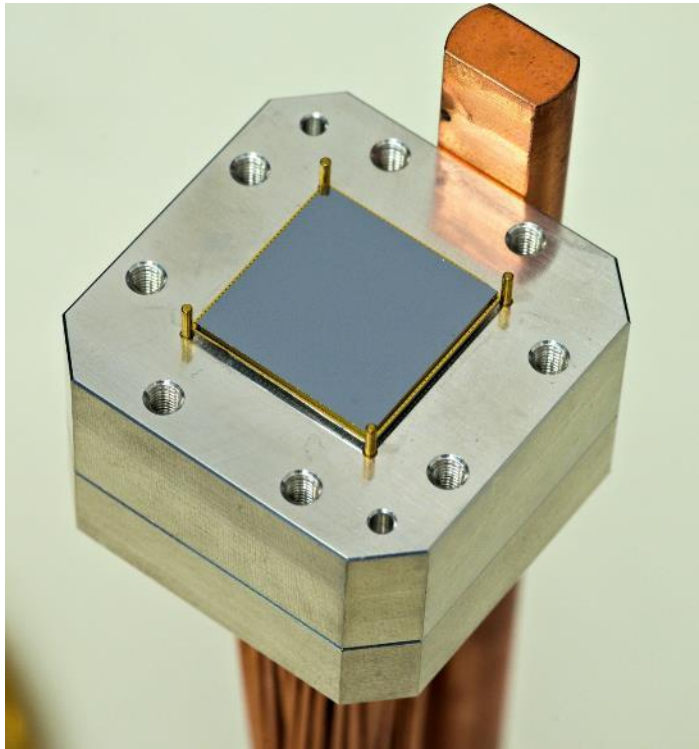




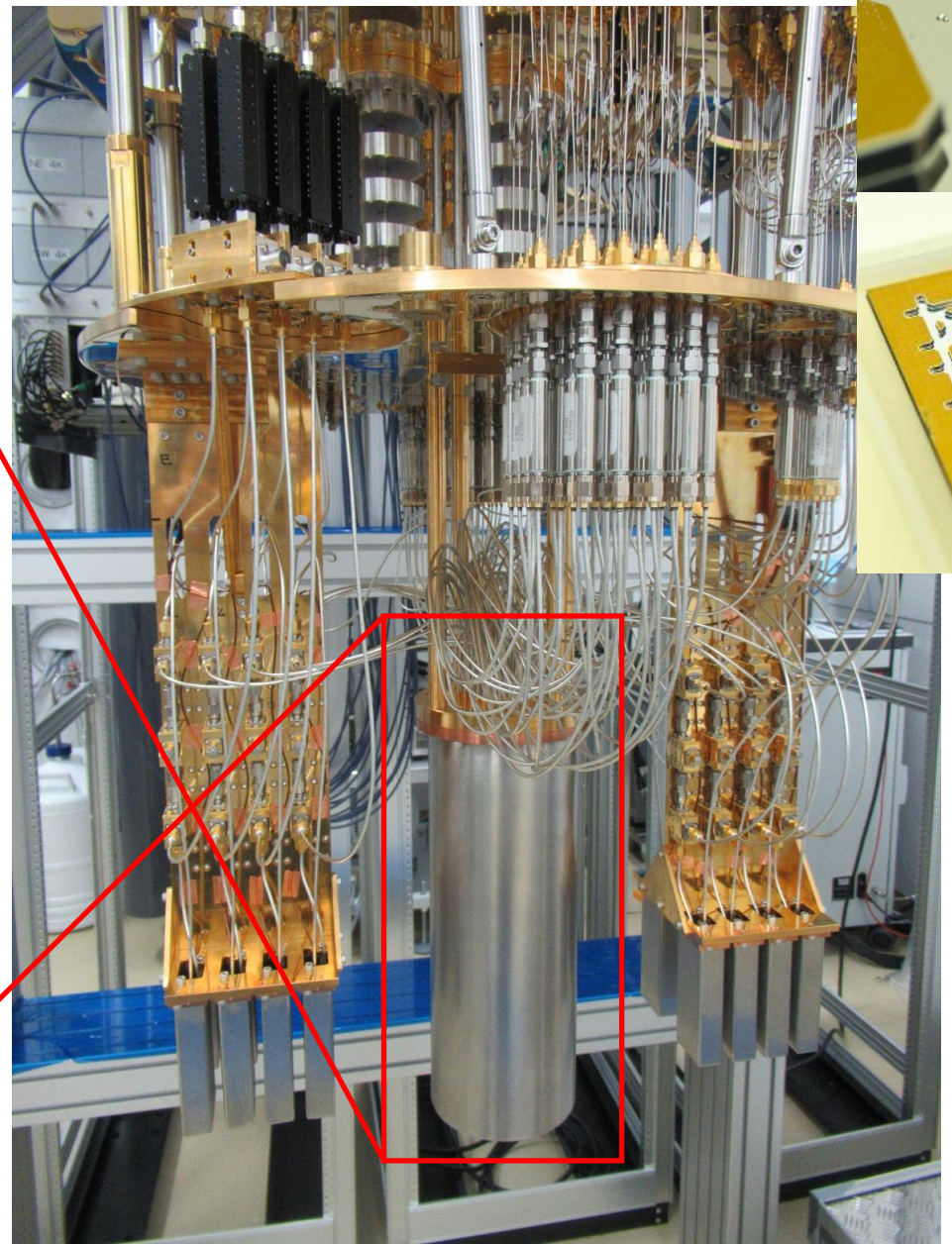
Sample package

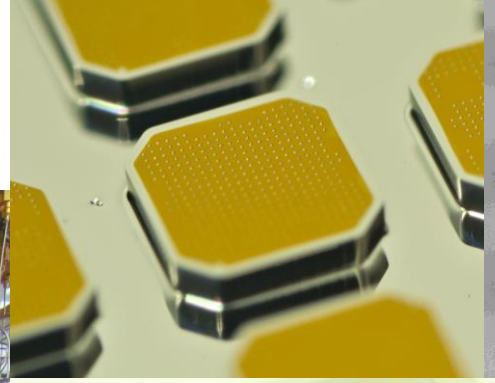


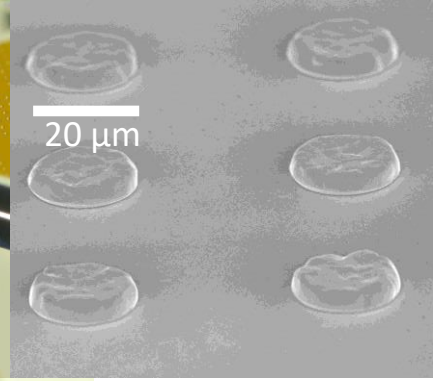


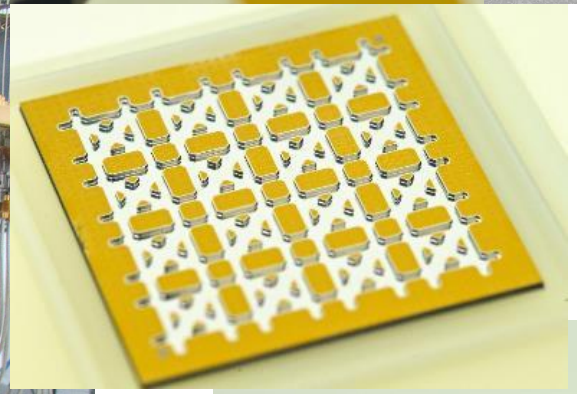


Sample package

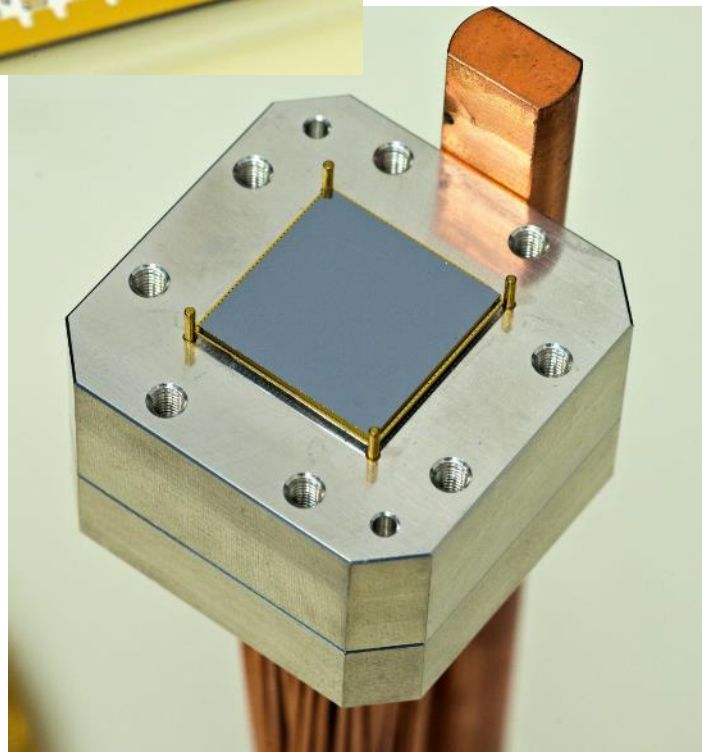






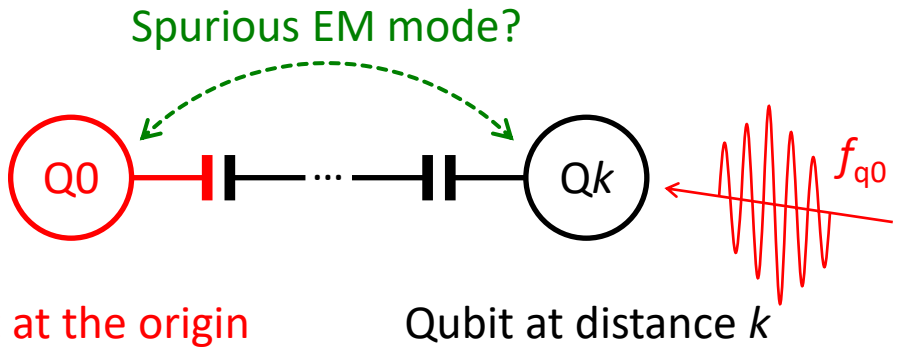


Cover chip with
Indium bumps

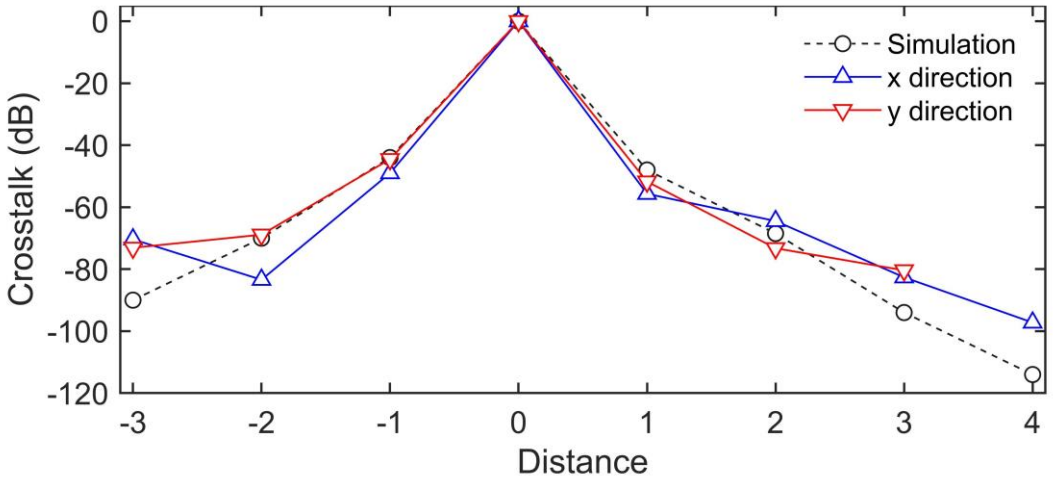


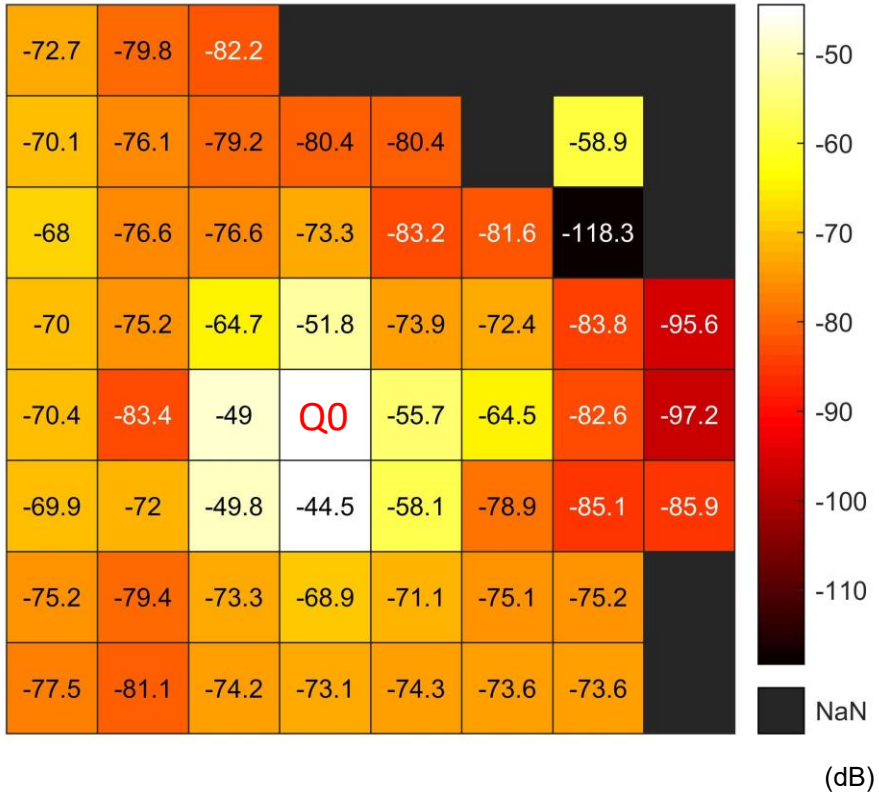
Control signal crosstalk

Characterized by **Shuhei Tamate**

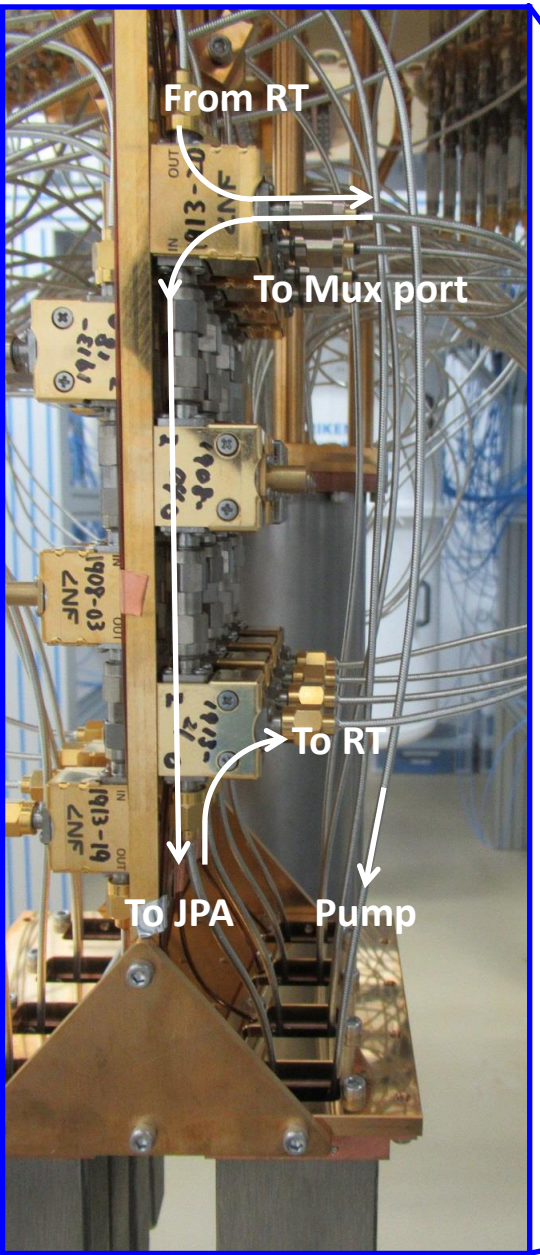


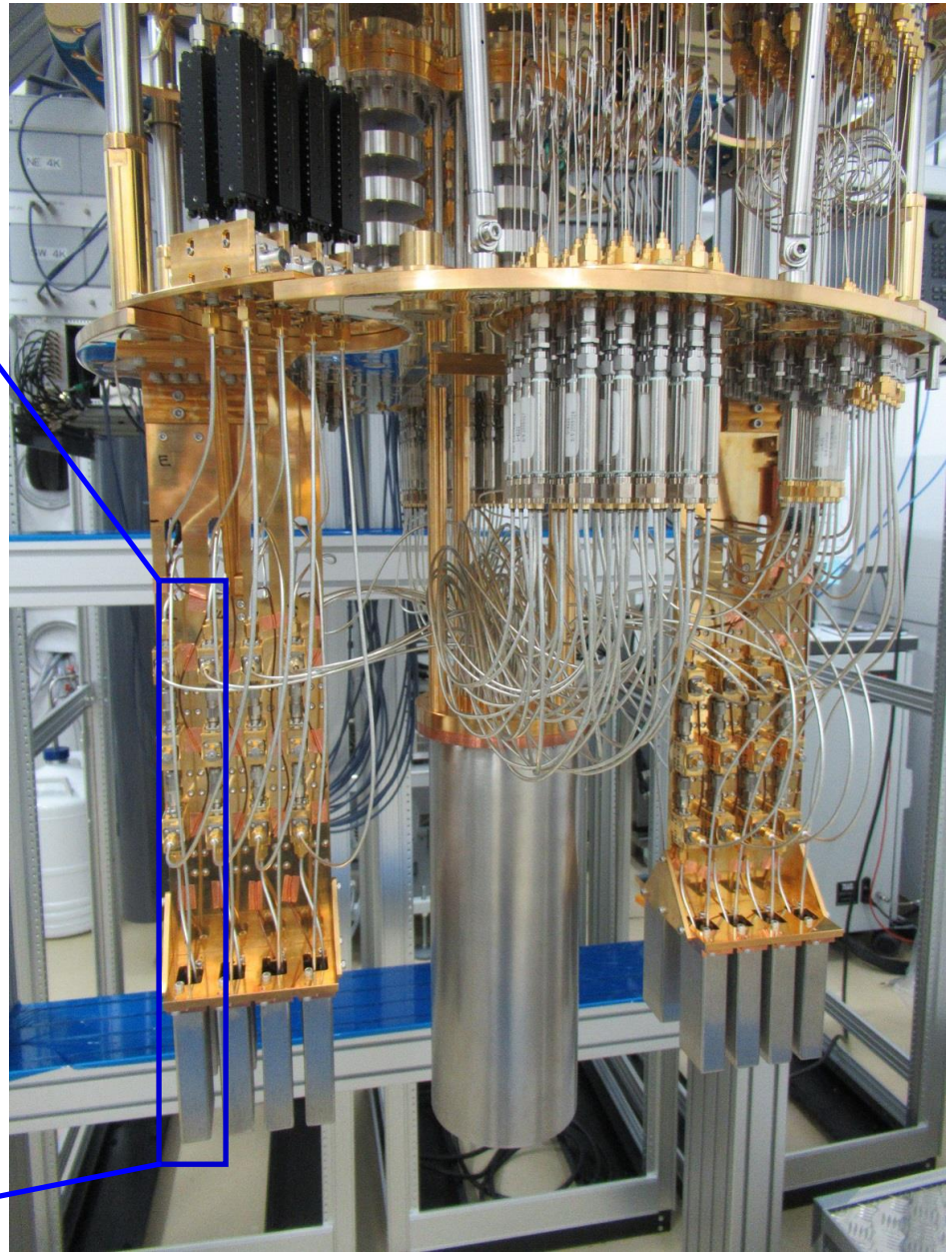
- Estimate the crosstalk from the Rabi frequency of 0-th qubit driven from k-th control port

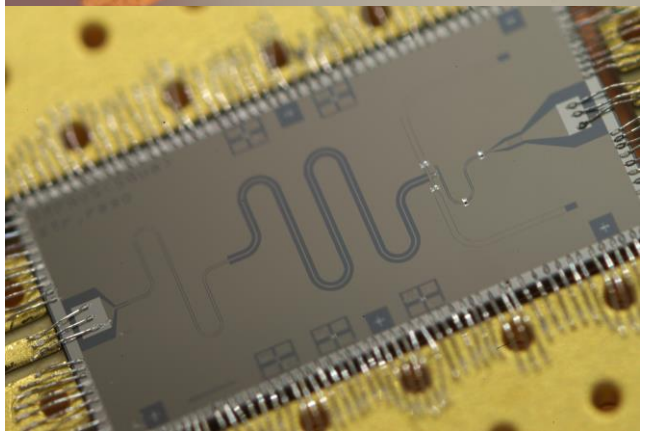


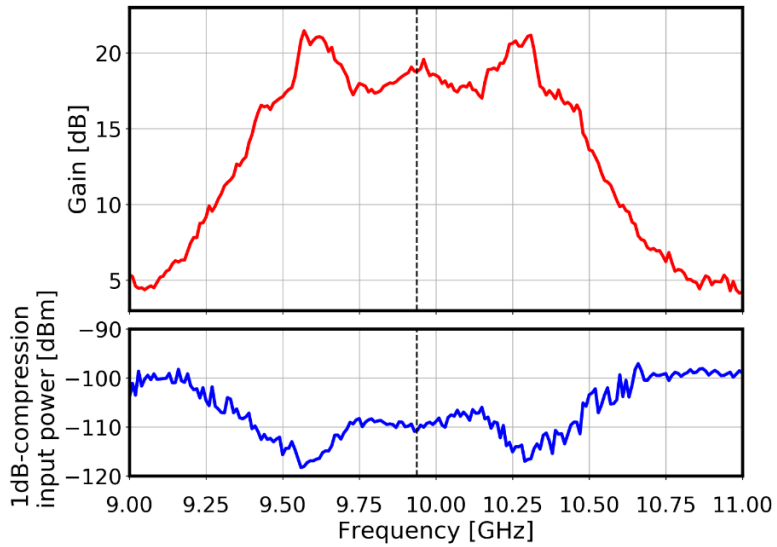


Josephson parametric amplifier



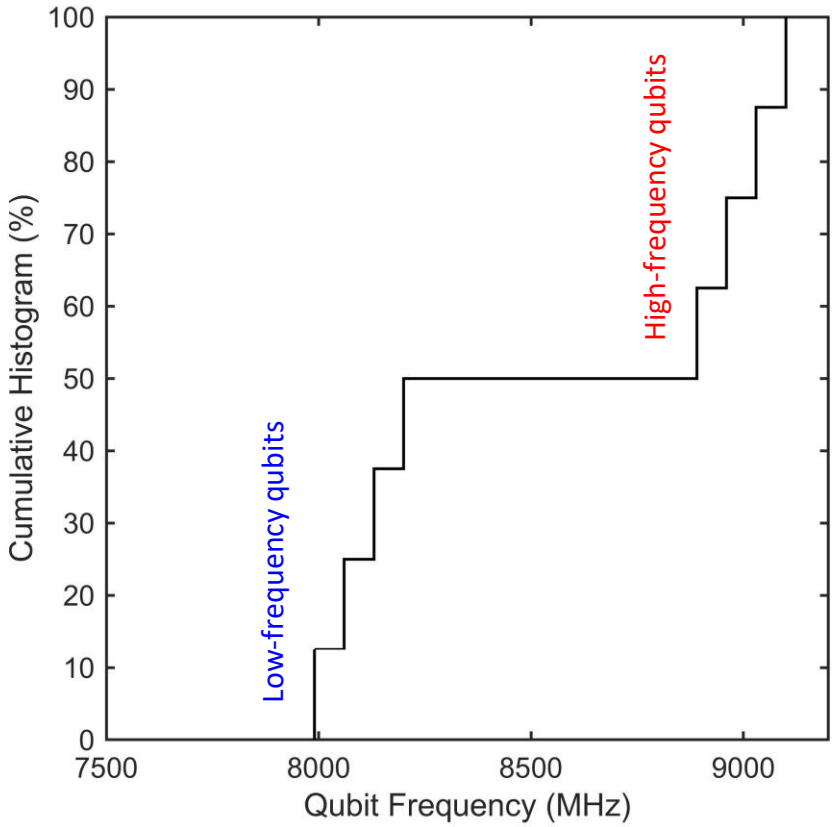


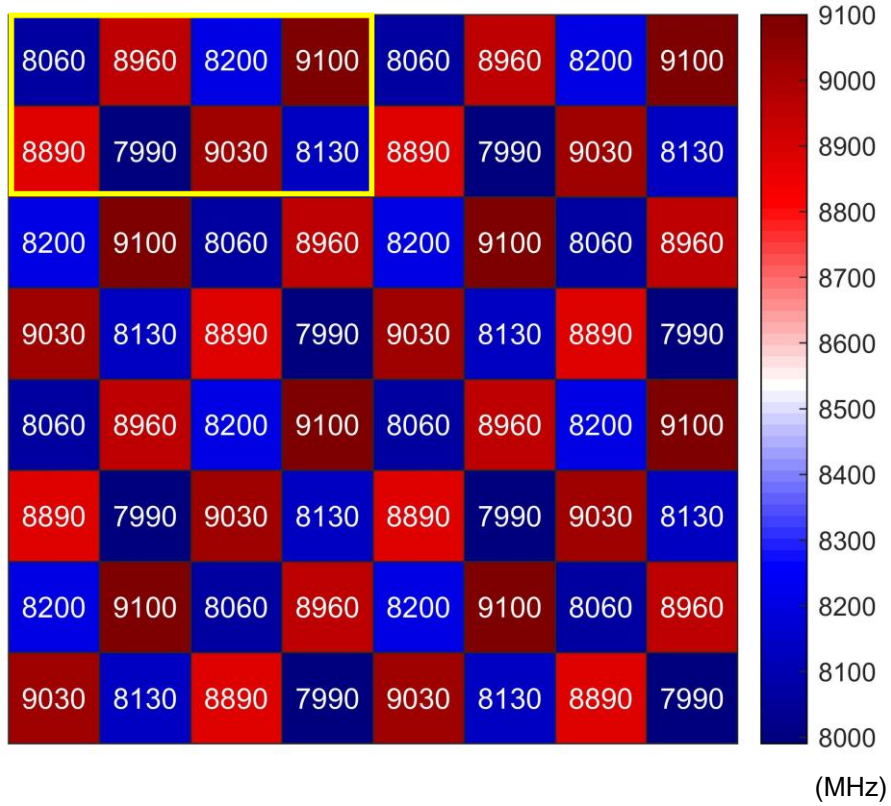




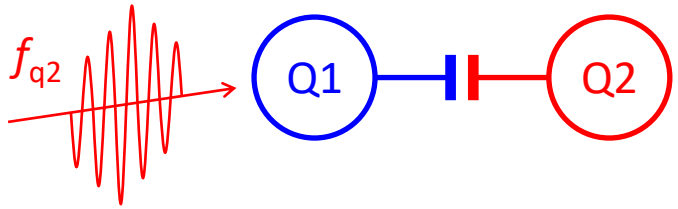
Qubit frequency distribution

Design values



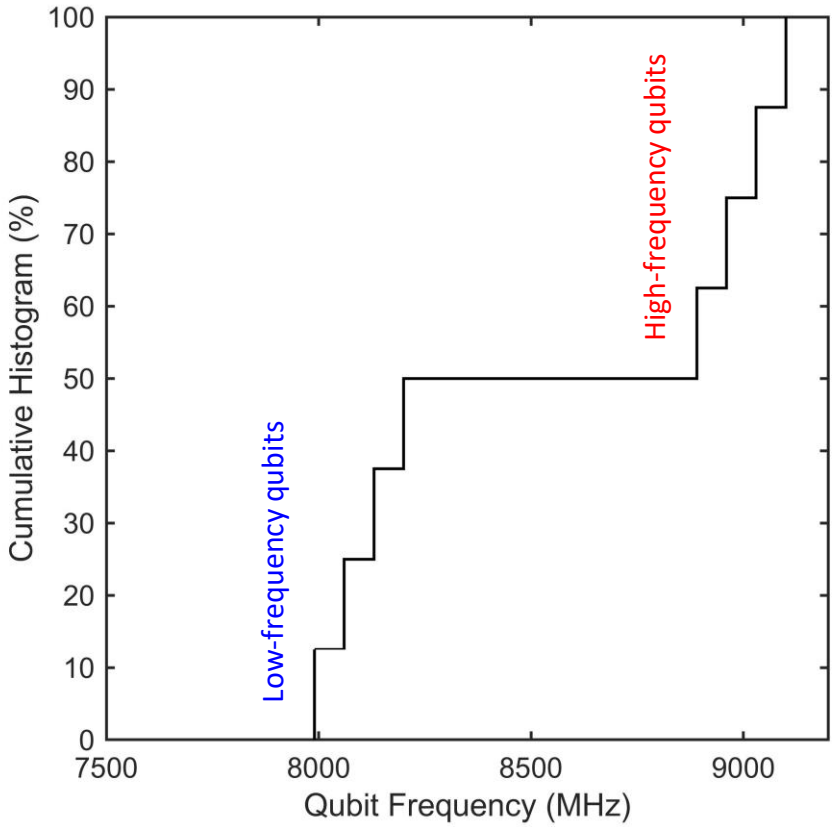


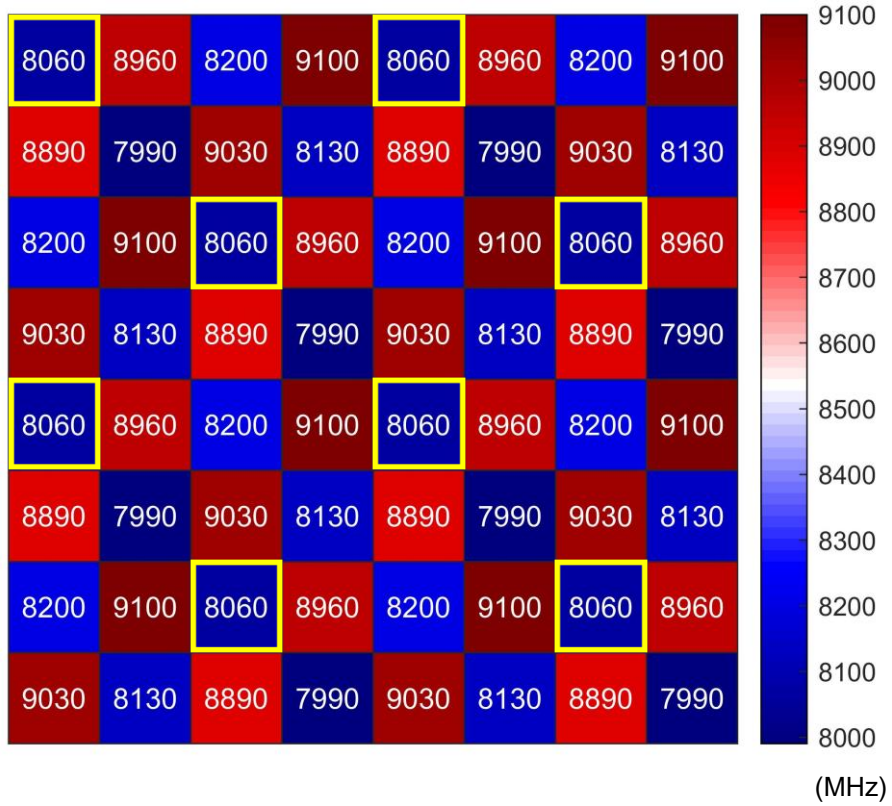
- Large detuning between nearest neighbors for CR gates
- Target variation **< 0.25%** to avoid frequency collisions



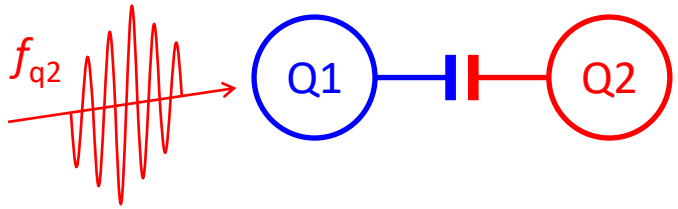
Qubit frequency distribution

Design values



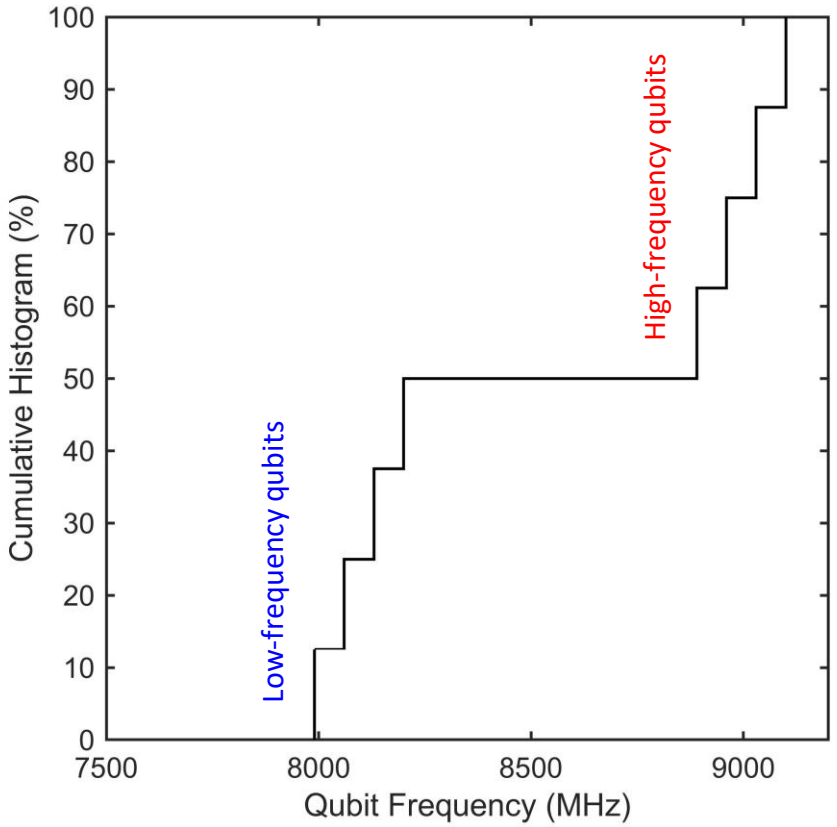


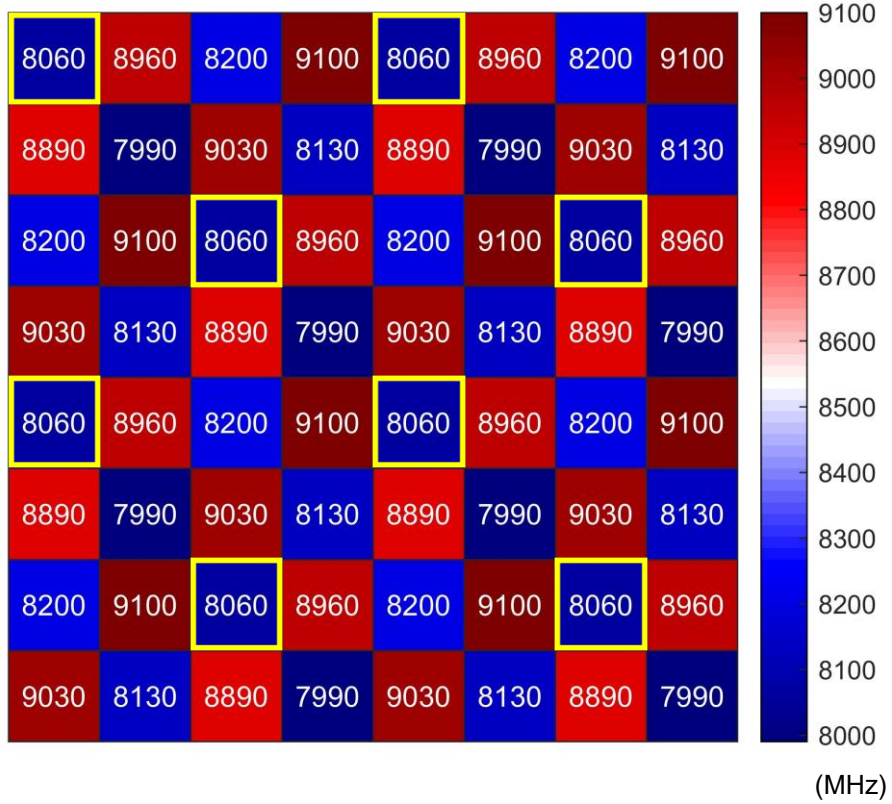
- Large detuning between nearest neighbors for CR gates
- Target variation **< 0.25%** to avoid frequency collisions



Qubit frequency distribution

Design values

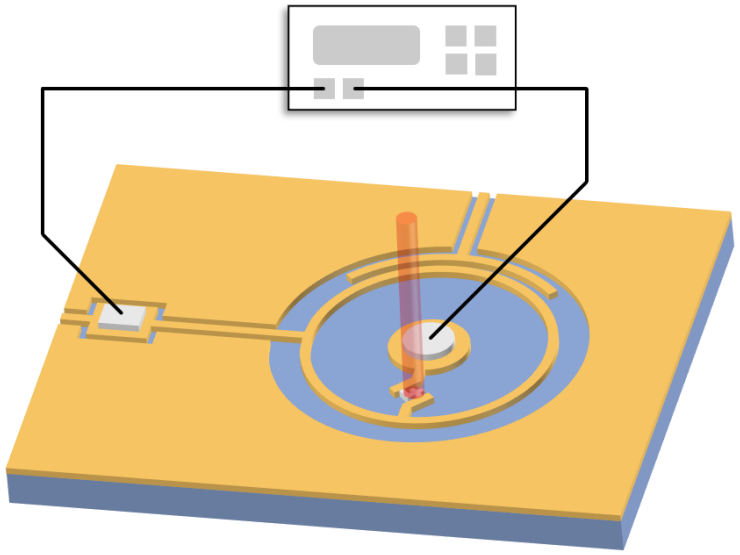


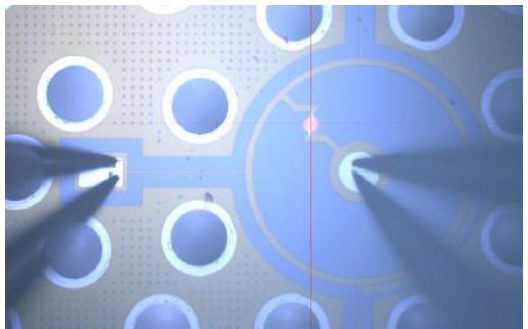


MAR-F18 (pervious seesion): Tue. March 18, 10:00am–10:12am **Shinichi Inoue** *et al.*
"Frequency-collision analysis for the scalable quantum computation based on high-intensity-driven all-microwave gates"

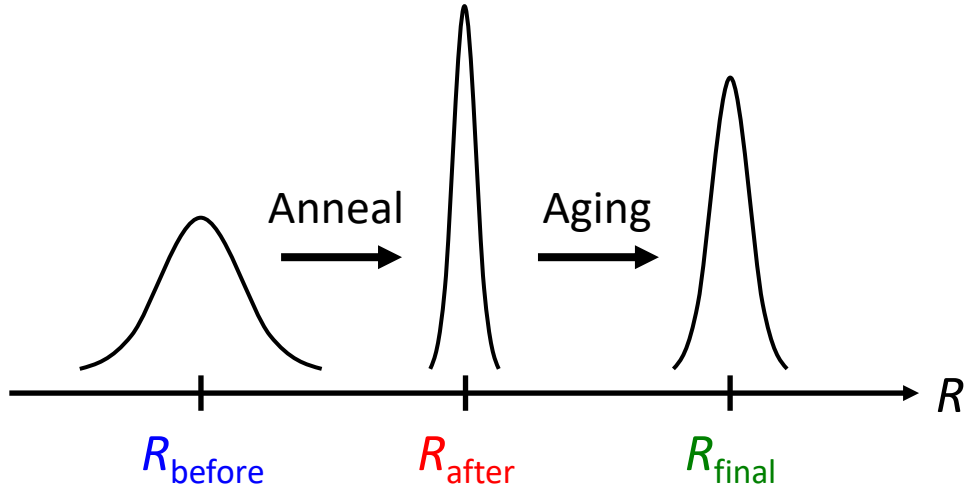
Laser annealing

- High-fidelity control of a lattice of **fixed-frequency transmons** requires **high-uniformity in the junction resistances** (particularly for CR gates)
- Laser annealing is a useful means for **post-fab resistance tuning**



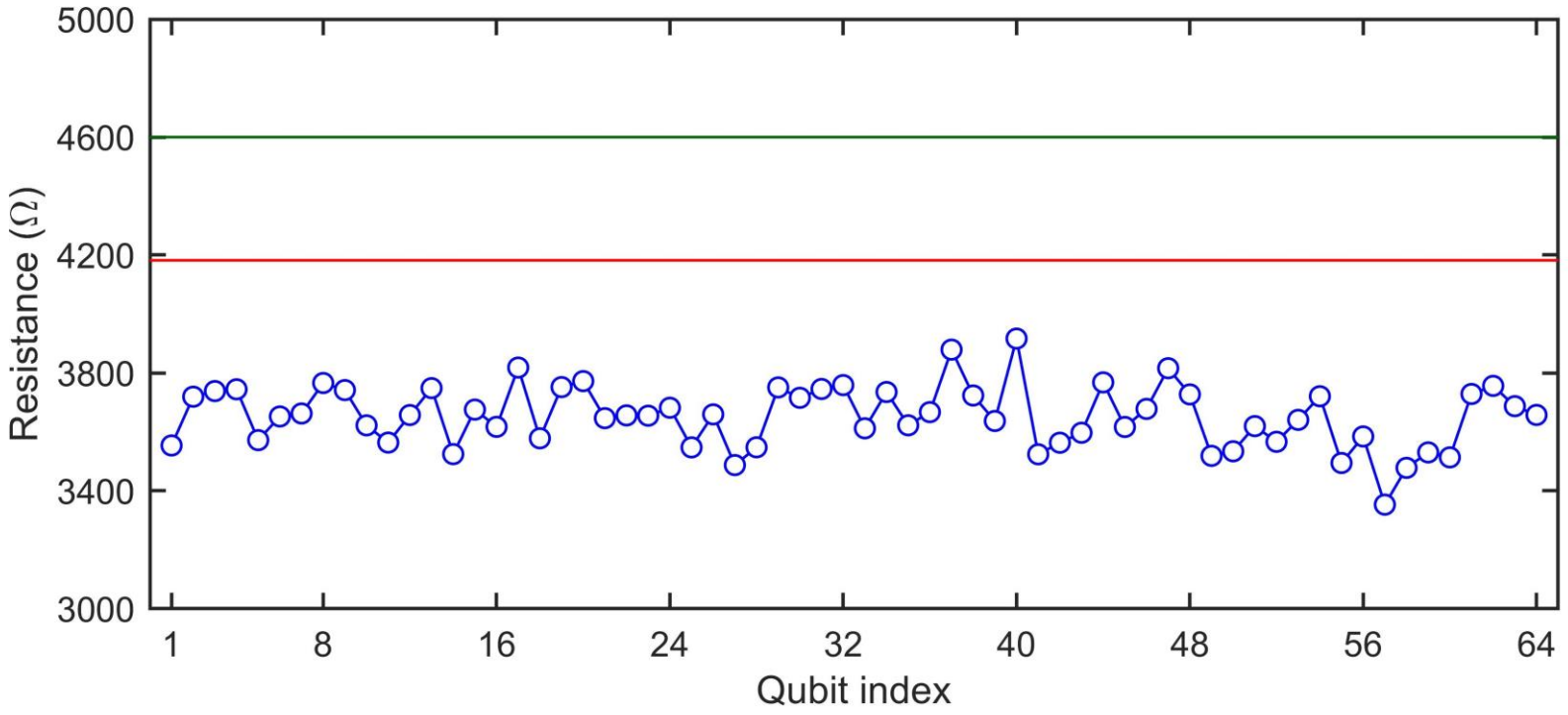


Distribution of junction resistance in a chip



Laser annealing

- Target R_{after} was determined from the expected 10% resistance increase due to aging



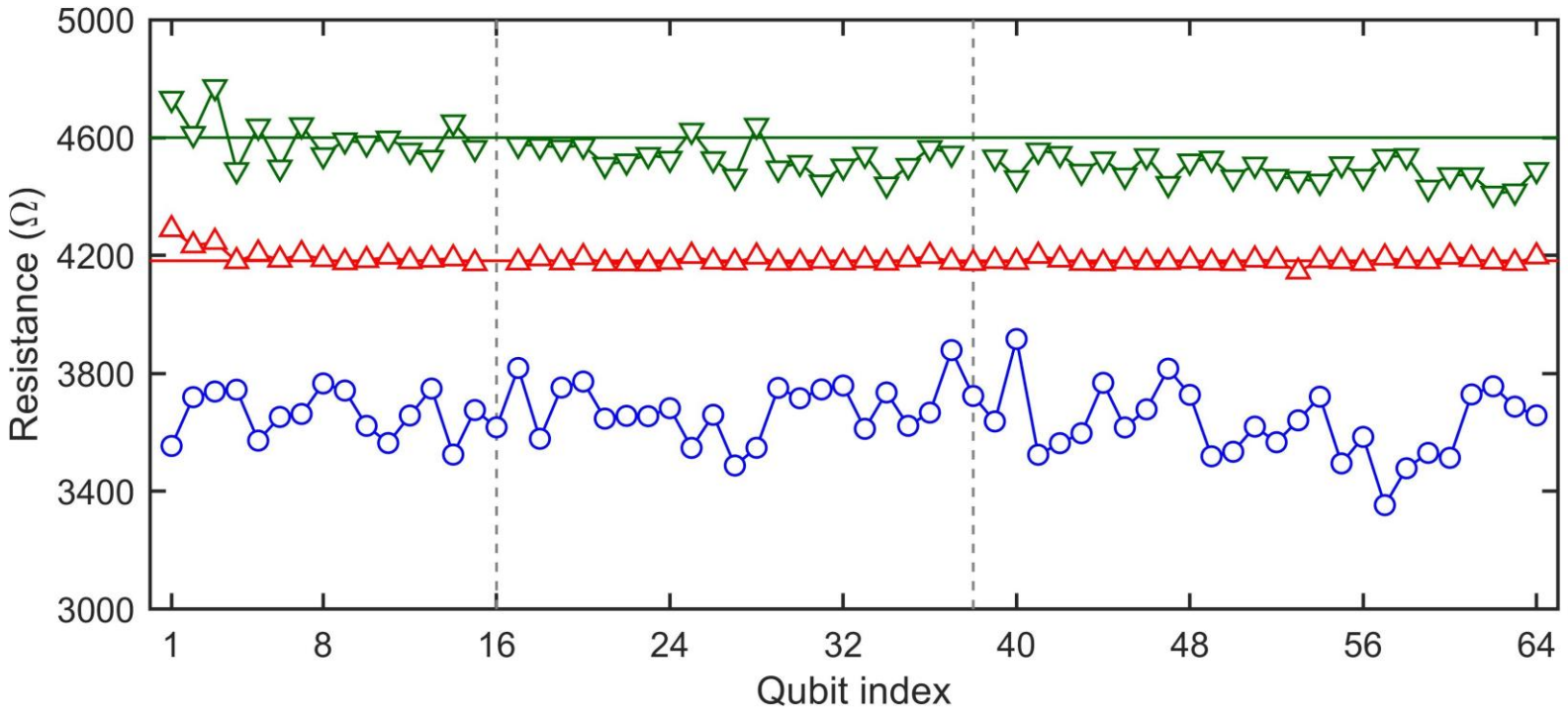
R_{final} (target: 4600 Ω = R_{after} x 1.1)

R_{after} (target: 4182 Ω)

R_{before} (avg.: 3653 Ω, r. std. dev.: 2.87%)

Laser annealing

- Target R_{after} was determined from the expected 10% resistance increase due to aging
- **Automated annealing** sequence took **8 hours** to complete a 64Q chip
- Additional **11 hours** for aging
- (Actively working on alternating bias assisted annealing in parallel)



R_{final} (avg.: 4530 Ω, r. std. dev.: 1.55%)

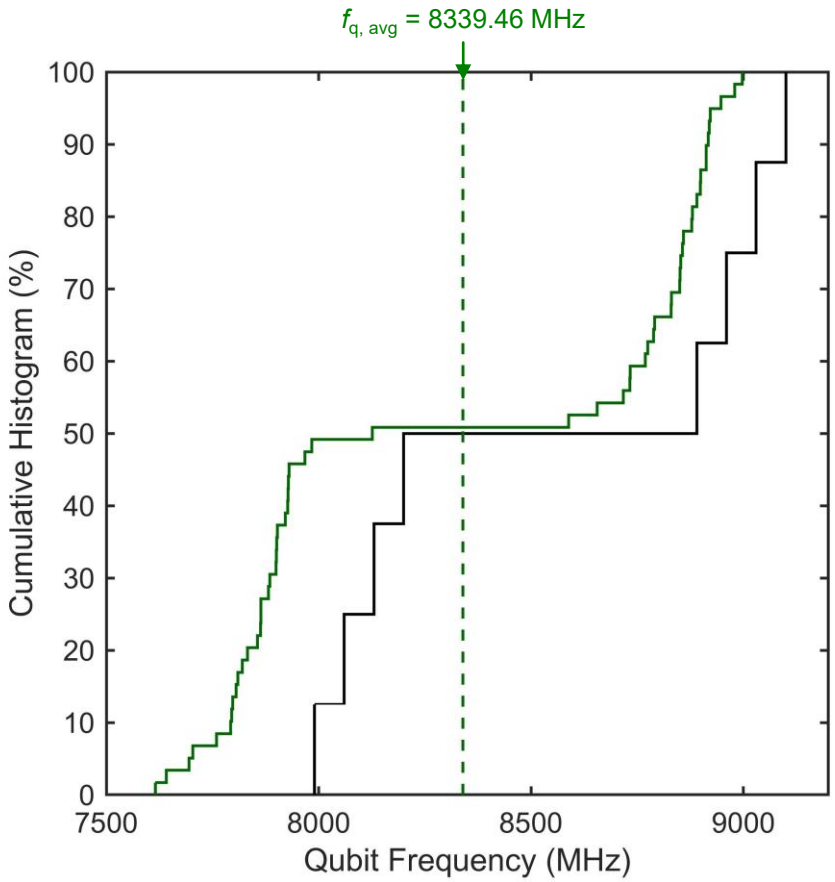
R_{after} (avg.: 4186 Ω, r. std. dev.: 0.46%)

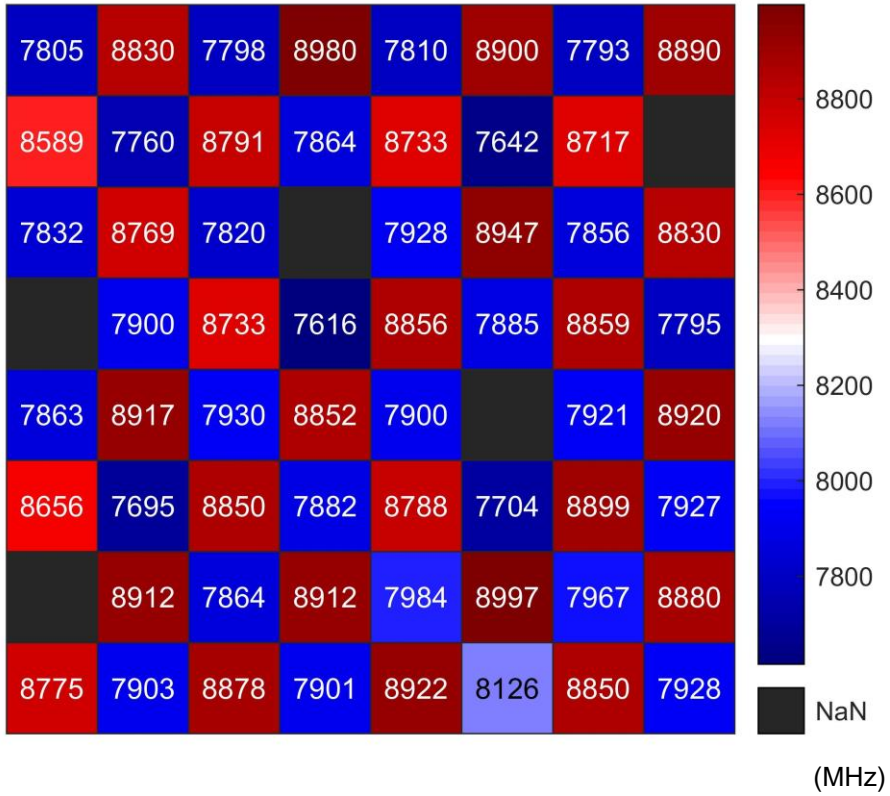
R_{before} (avg.: 3653 Ω, r. std. dev.: 2.87%)

Qubit frequency distribution

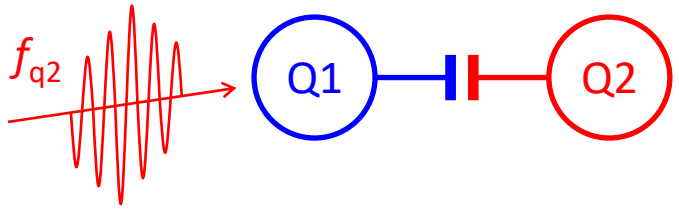
Characterized by **Shiyu Wang**

Measured values



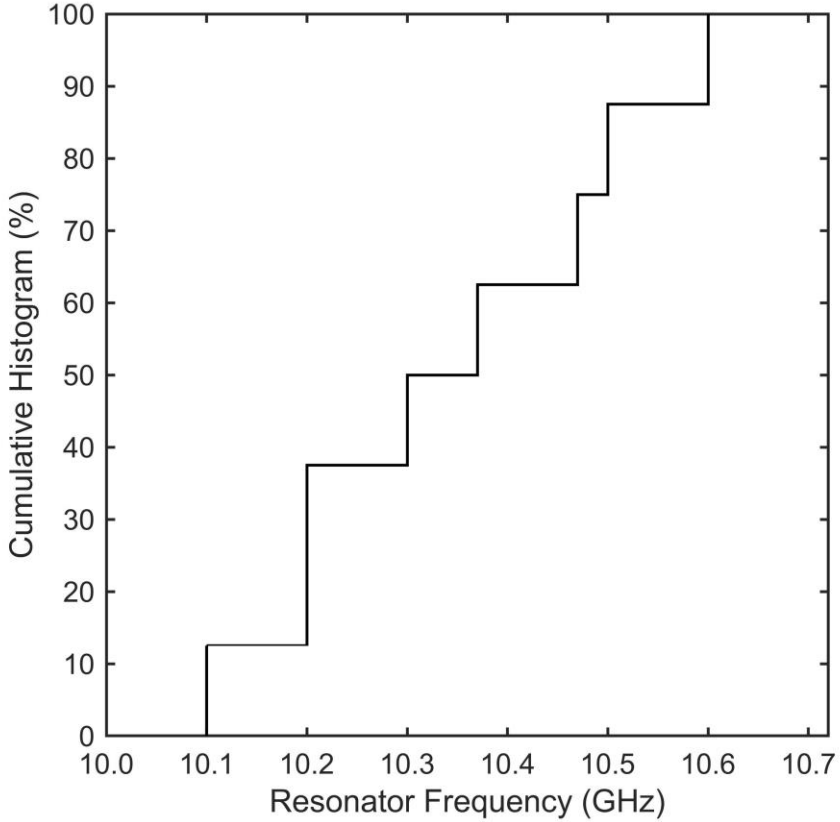


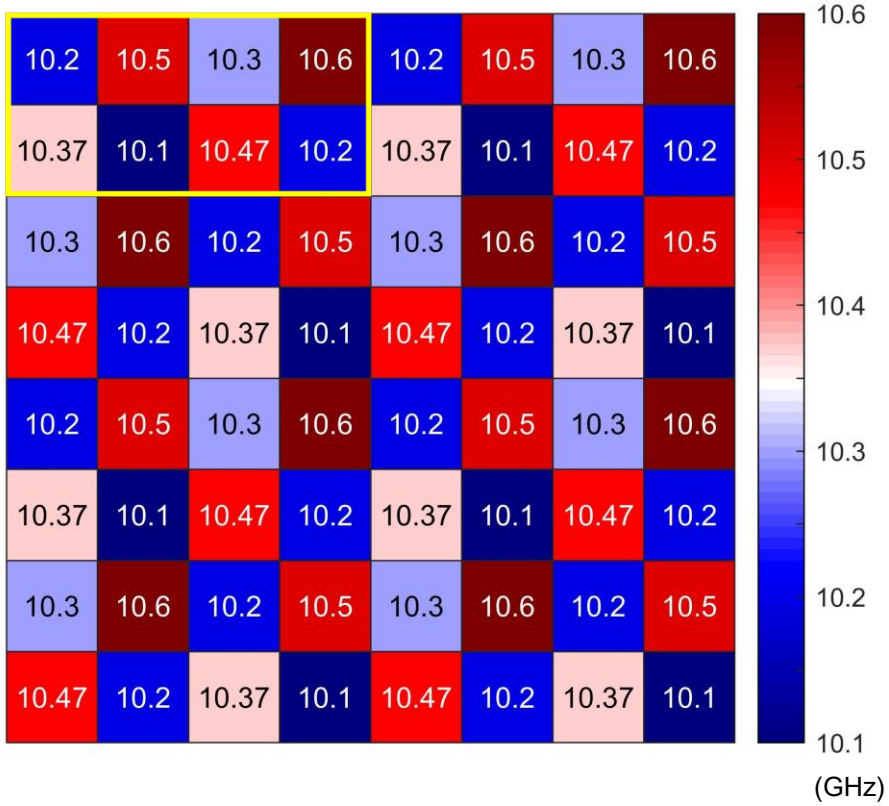
- R. std. dev. of 8 types of qubits: 0.69%, 0.44%, 1.18%, 1.48%, 0.95%, 0.82%, 0.82%, 1.14%



Resonator frequency distribution

Design values



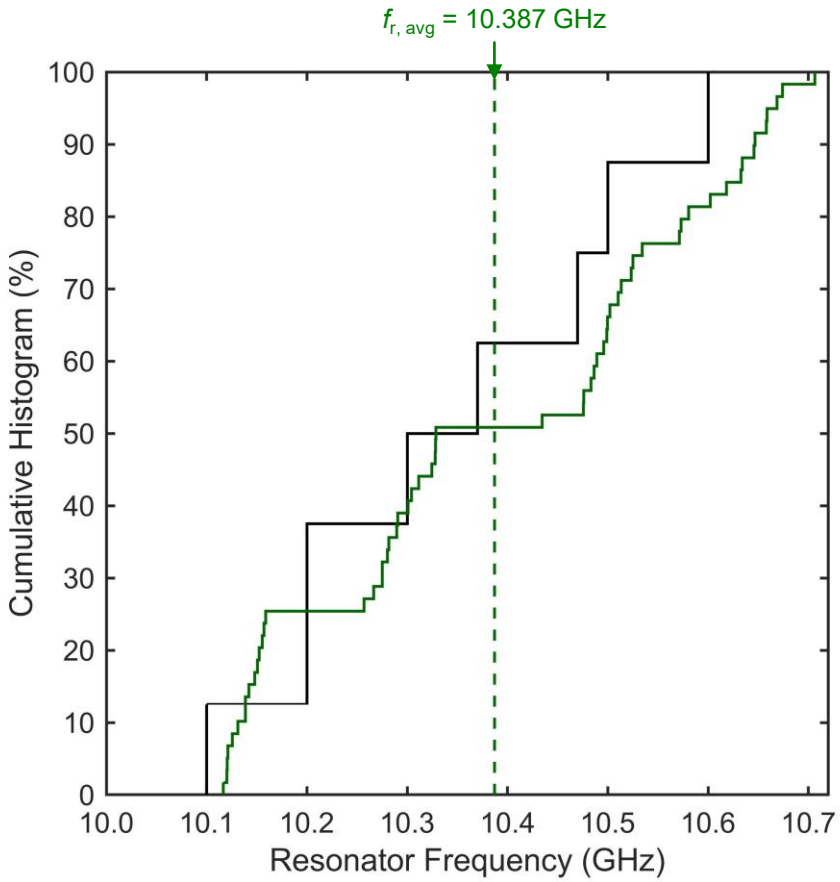


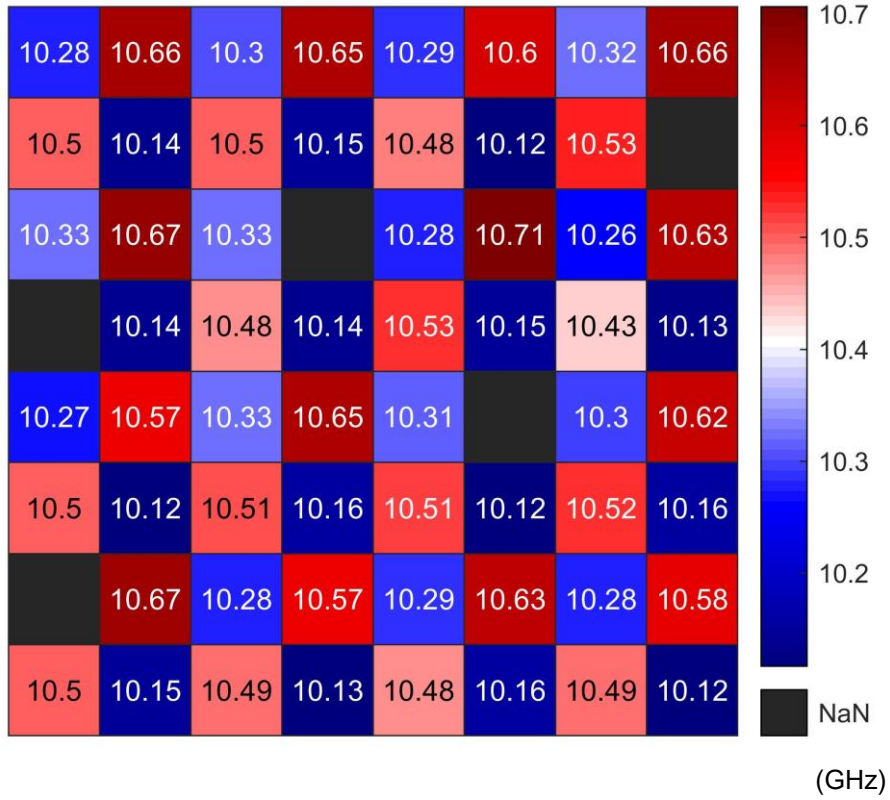
- Resonators in the same unit (sharing the same Mux port) must be differentiated

Resonator frequency distribution

Characterized by **Shiyu Wang**

Measured values

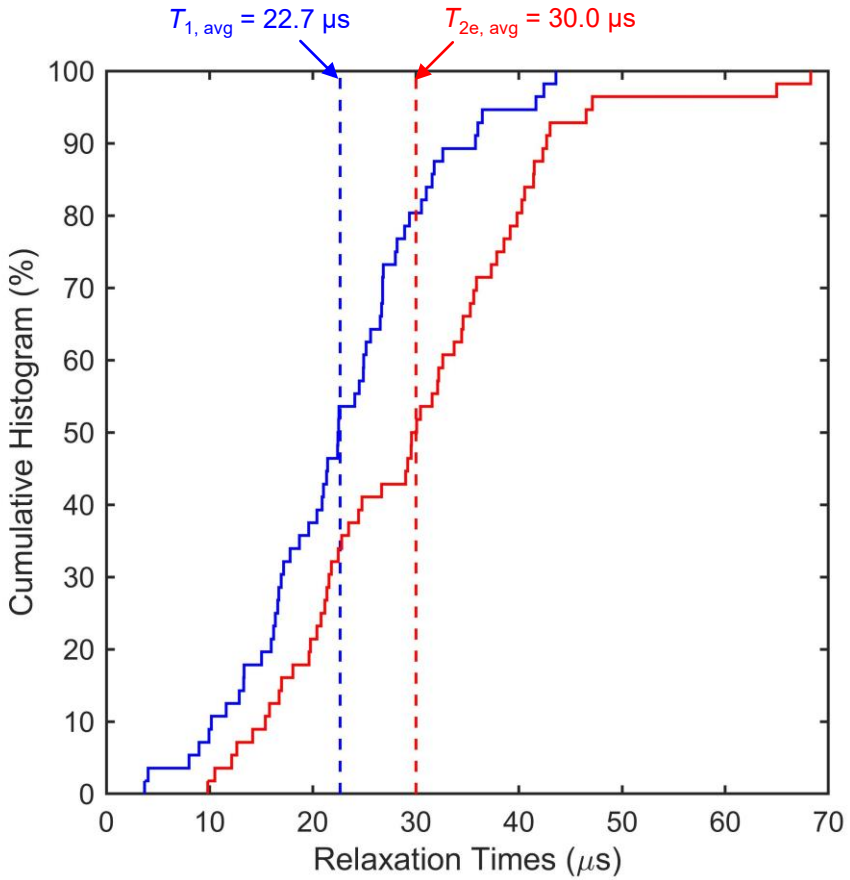




- R. std dev. of 8 types of resonators: 0.23%, 0.34%, 0.22%, 0.09%, 0.18%, 0.26%, 0.19%, 0.07%

Relaxation times & fidelities

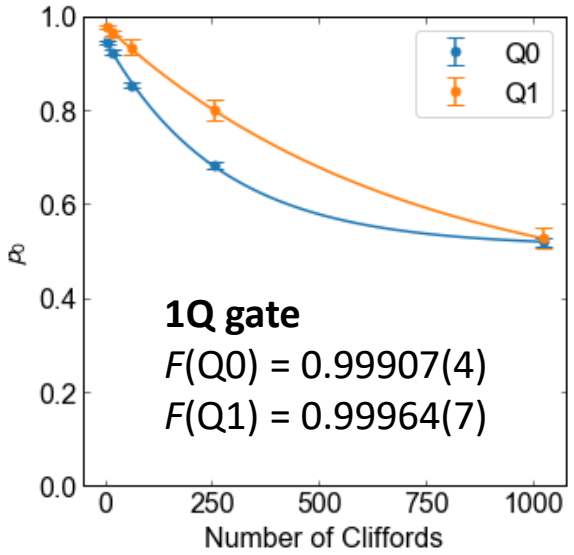
Characterized by **Shiyu Wang**

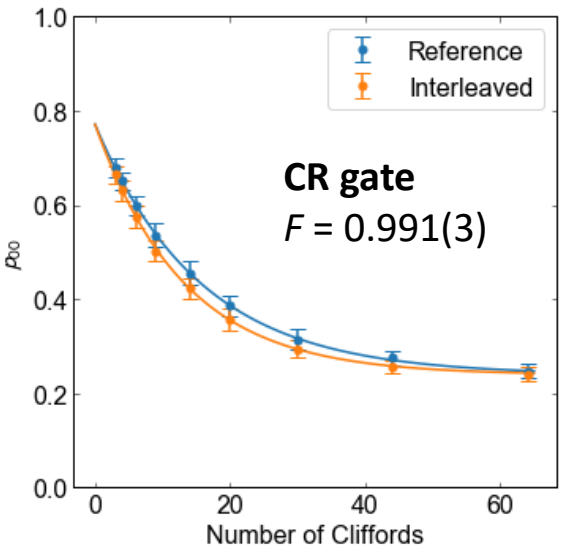


- Longest T_1 = 43.6 μs, T_{2e} = 68.3 μs

Best values

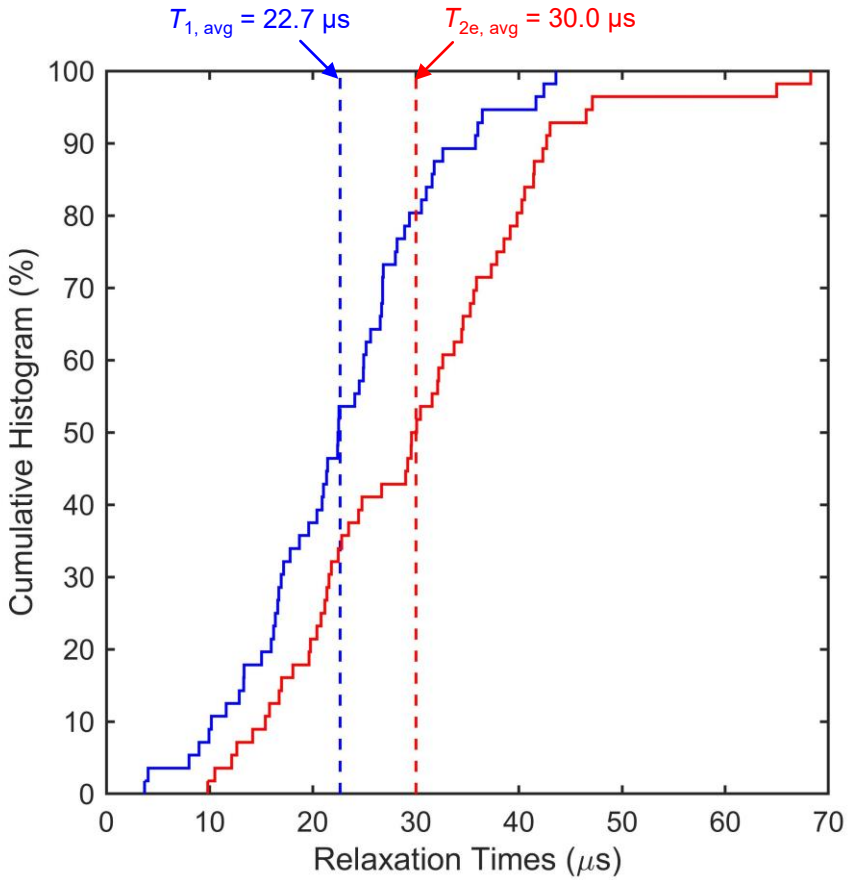
- Relaxation times: $T_1 \approx 90$ μs, $T_{2e} \approx 100$ μs (@8 GHz)
- 1Q gate: F = 99.96% (17 ns)
- CR gate: F = 99.1% (170 ns)
- Readout: F = 99.91% (56 ns)





Relaxation times & fidelities

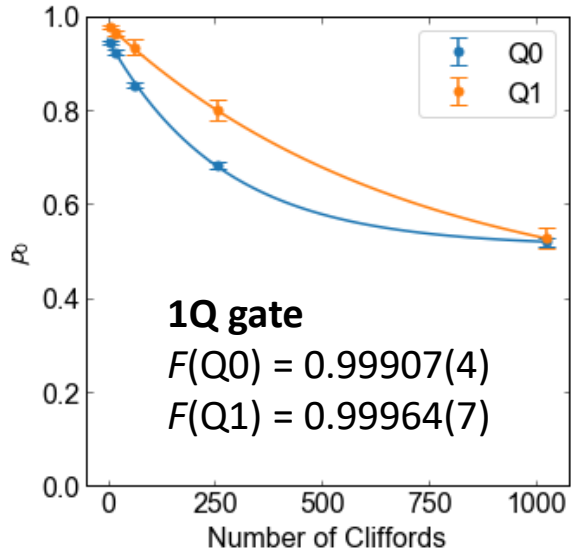
Characterized by **Shiyu Wang**

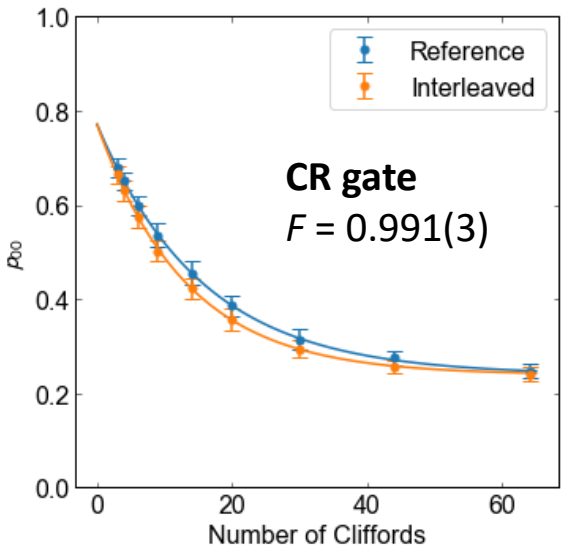


- Longest T_1 = 43.6 μs, T_{2e} = 68.3 μs

Best values

- Relaxation times: T_1 ≈ 90 μs, T_{2e} ≈ 100 μs (@8 GHz)
- 1Q gate: F = 99.96% (17 ns)
- CR gate: F = 99.1% (170 ns)
- **Readout: F = 99.91% (56 ns) → Peter Spring** *et al.*

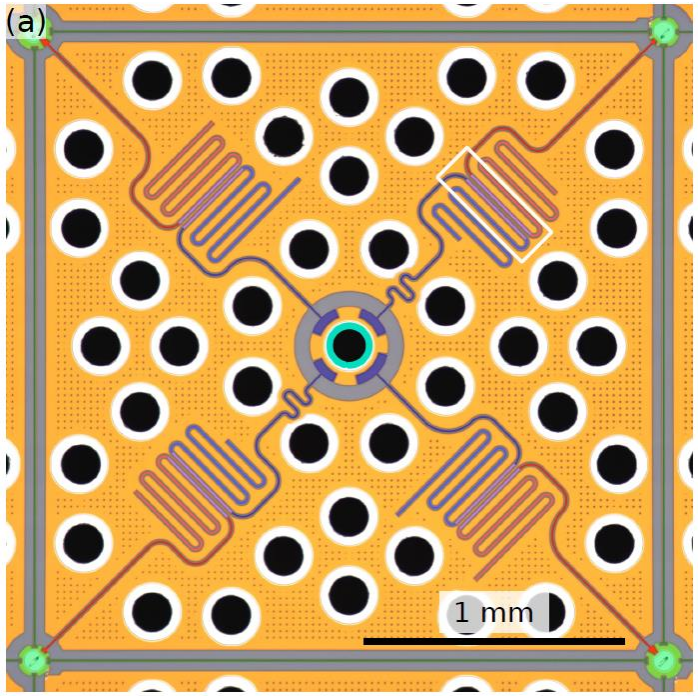


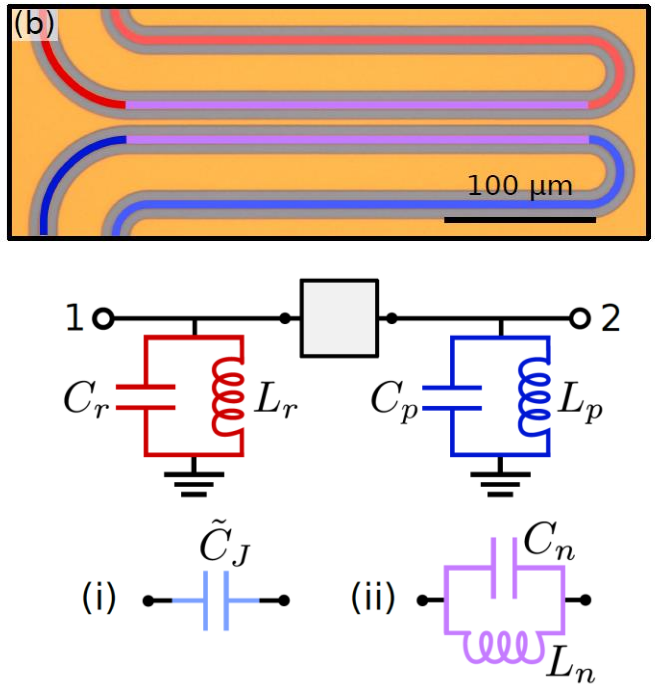


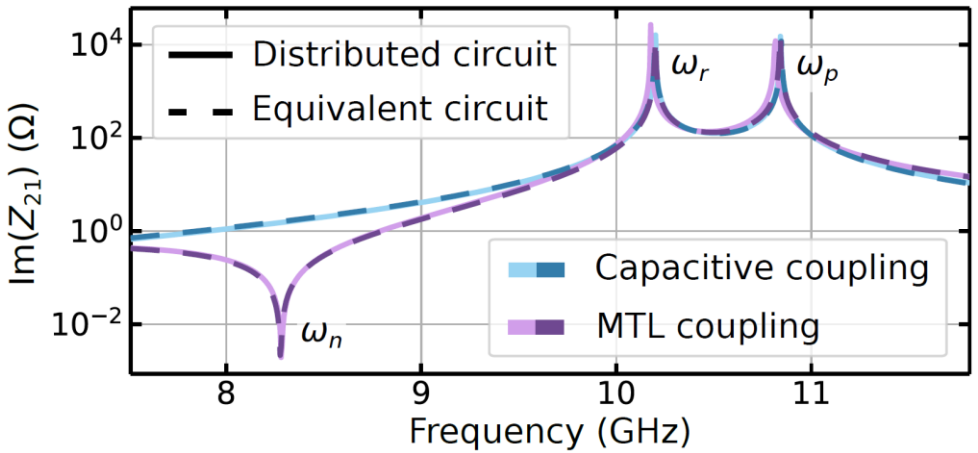
Fast readout with intrinsic Purcell filtering

arXiv:2409.04967 **P. A. Spring** *et al.*
MAR-L14: Wed. March 19, 8:00am–8:36am **Peter A. Spring**
"Fast multiplexed superconducting qubit readout with high assignment fidelity"

- Couple two λ/4 **readout** and **filter** resonators via a **proximitized section**
- Model as either distributed or equivalent circuit
- **Notch effect** not available by direct capacitive coupling



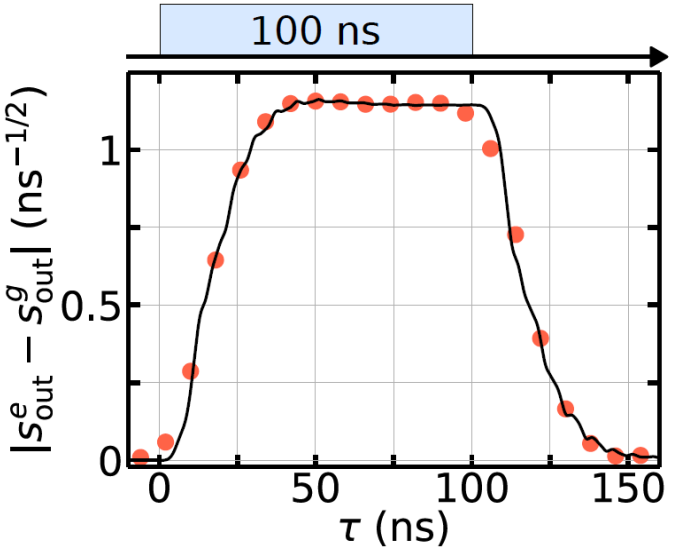


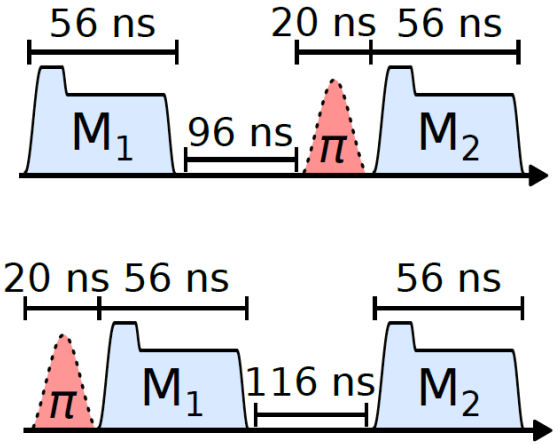


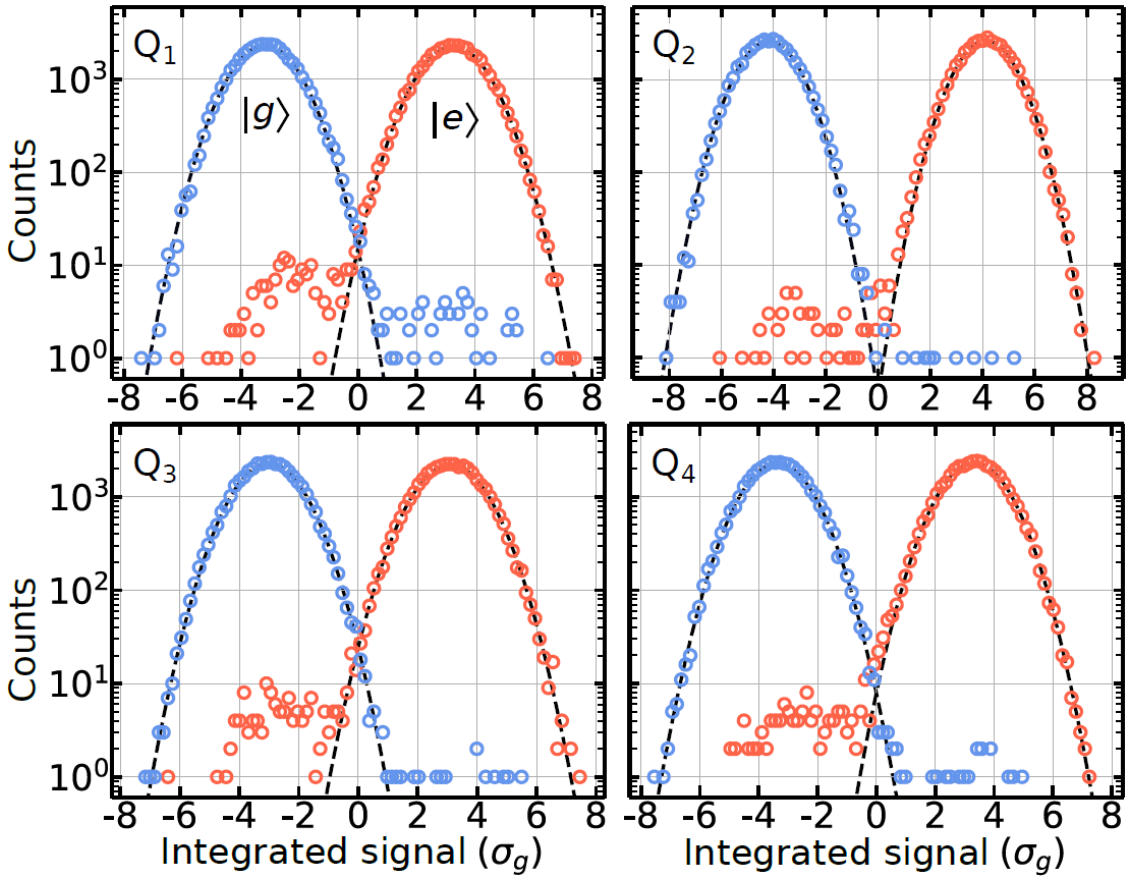
Fast readout with intrinsic Purcell filtering

arXiv:2409.04967 **P. A. Spring** *et al.*
MAR-L14: Wed. March 19, 8:00am–8:36am **Peter A. Spring**
"Fast multiplexed superconducting qubit readout with high assignment fidelity"

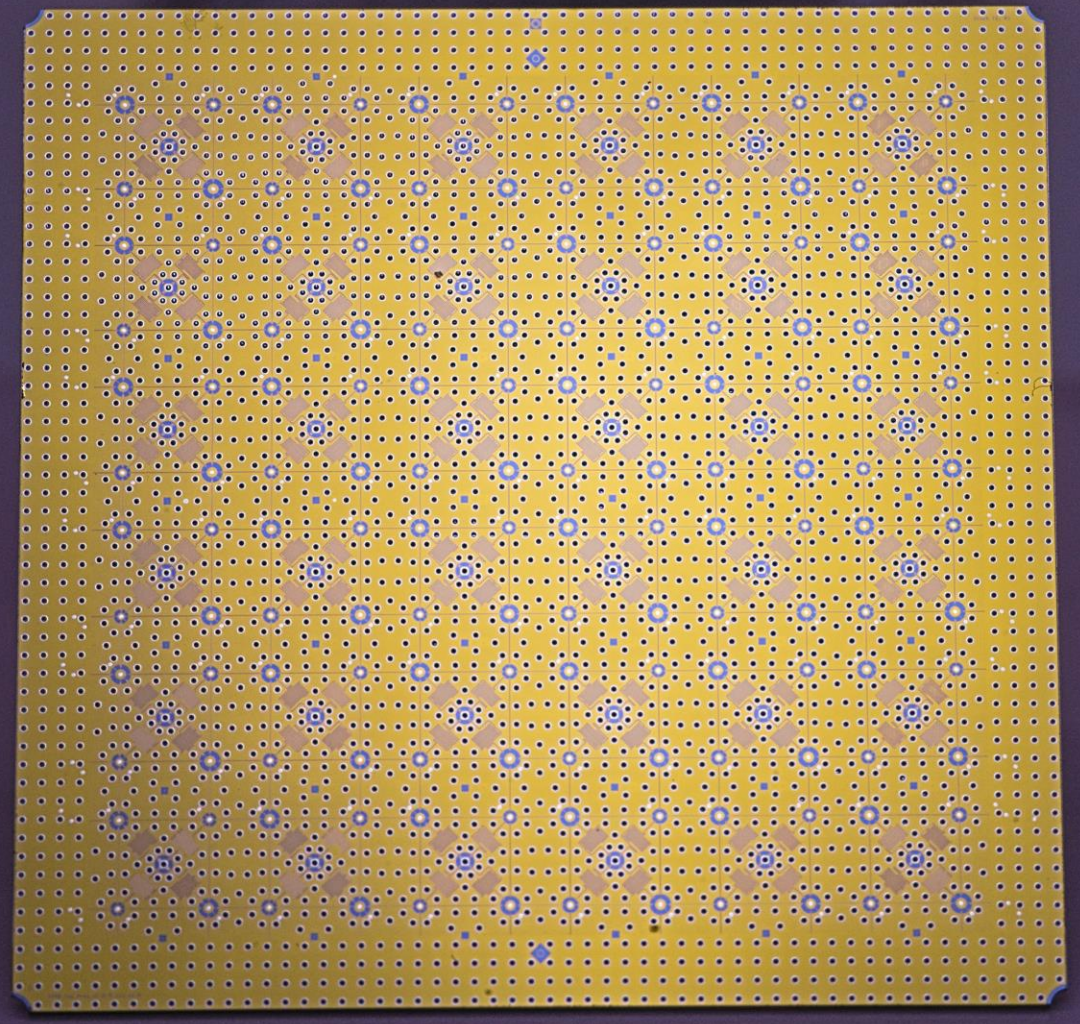
- State discrimination in 50 ns
- Simultaneous single-shot readout in **56 ns integration window**
- Average fidelity 99.77%, **highest 99.91%**

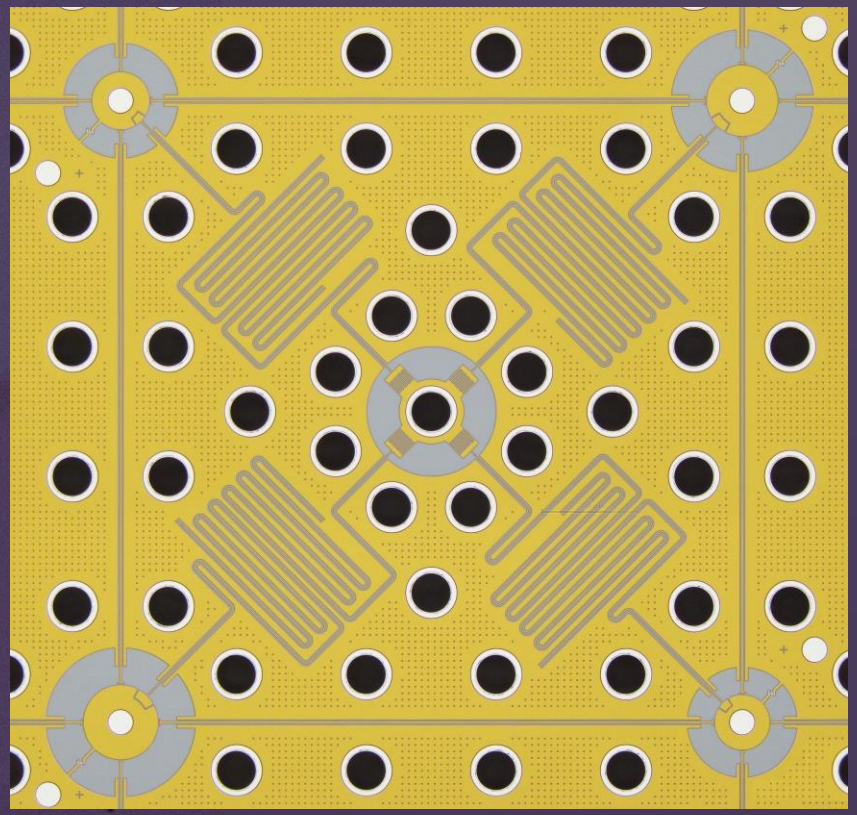






144Q chip





Frequencies

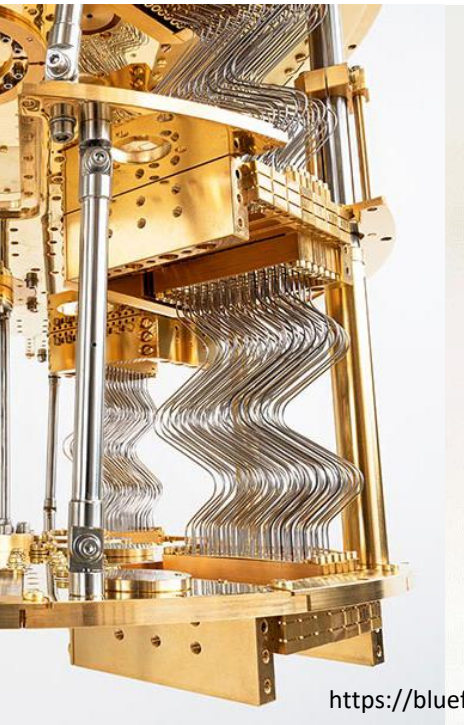
- f_q = 4.8–5.3 GHz
- f_r = 6.2–6.5 GHz
- f_p = 7.5–8.0 GHz

144Q system

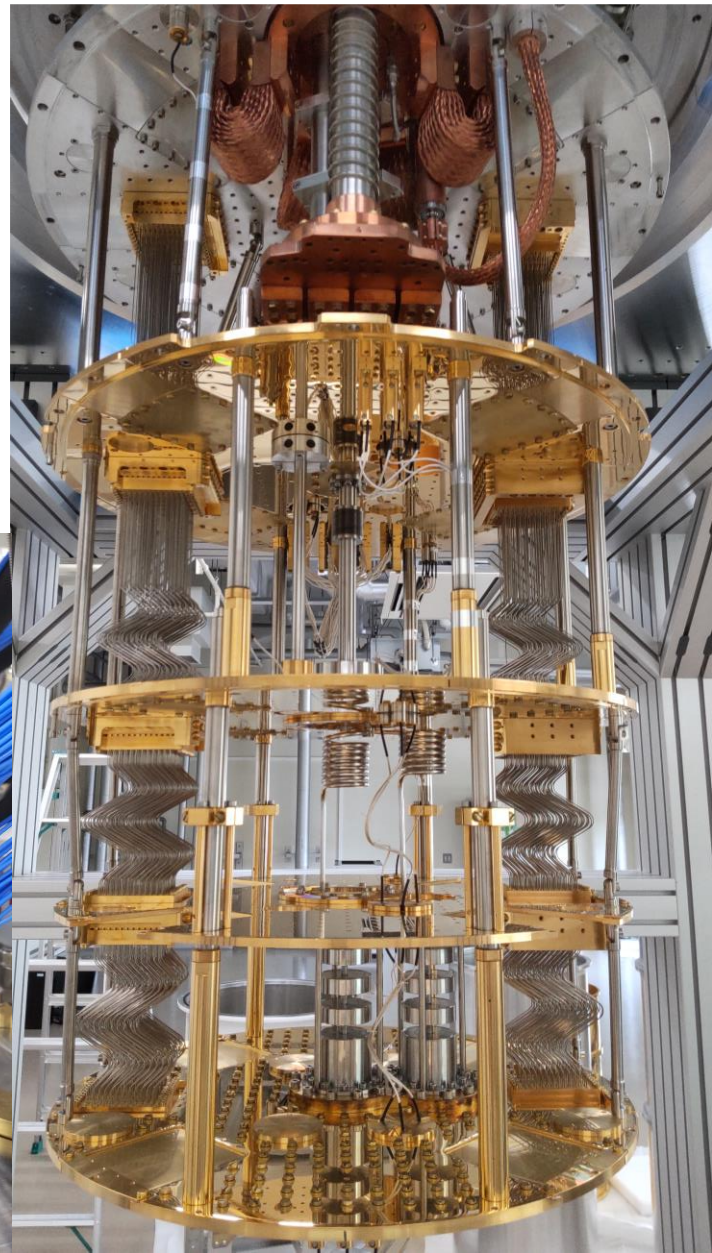
Need for 144Q

- 216 input lines (= 144 for control + 36 for readout + 36 for JTWPAs + 0 DC)
- 36 output lines

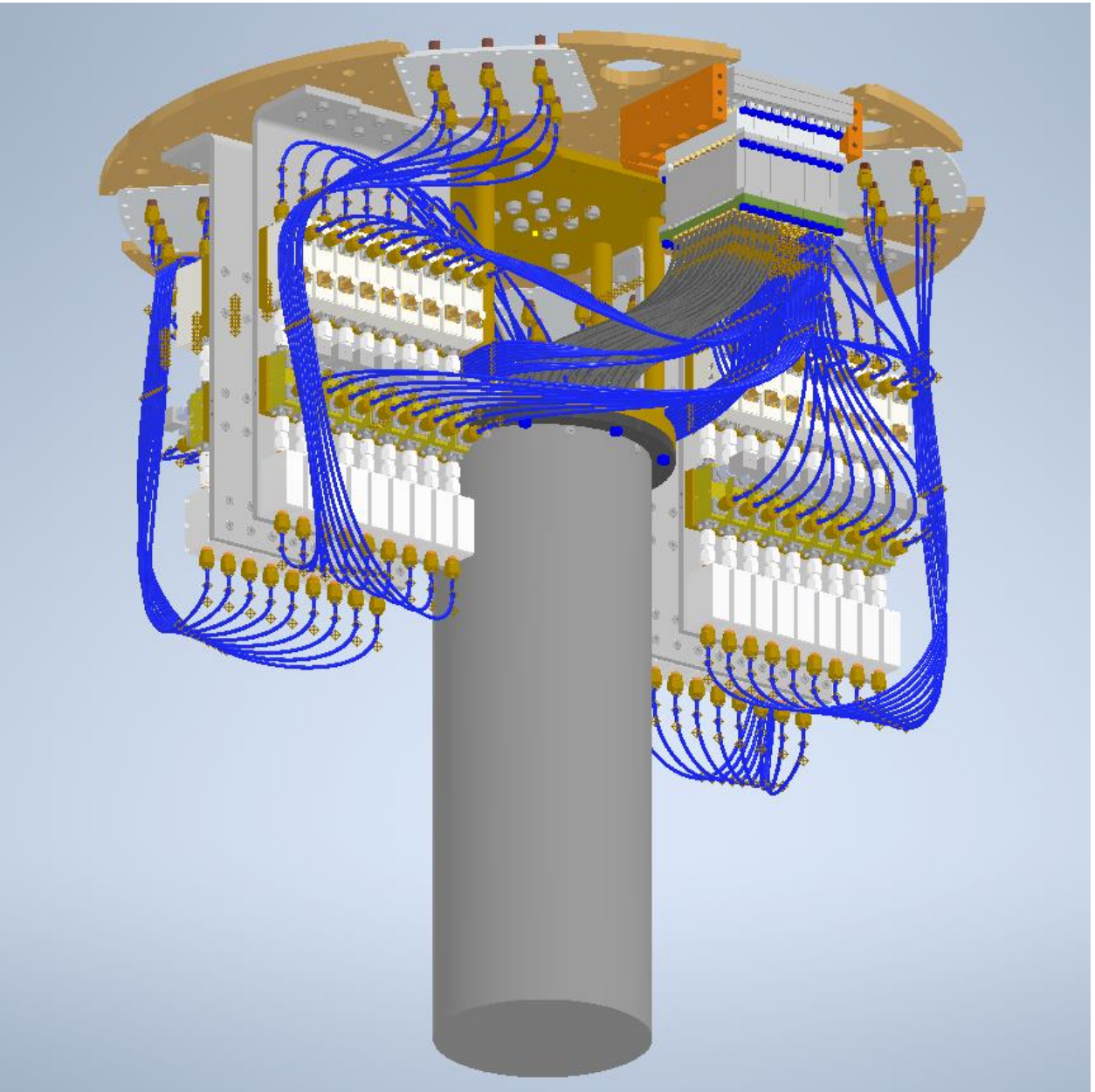
- High-density wiring while keeping the fridge size
  - 2 LOS ports can cover the input lines
  - 4 LOS ports for the output lines with bulky components



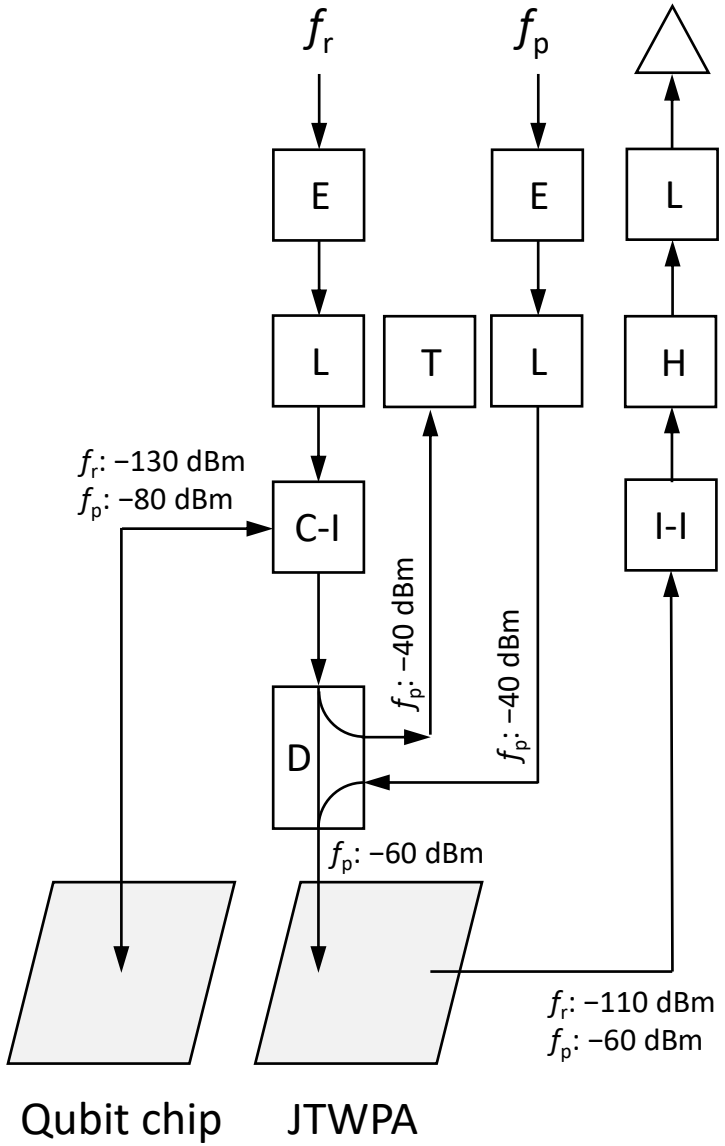
https://bluefors.com/



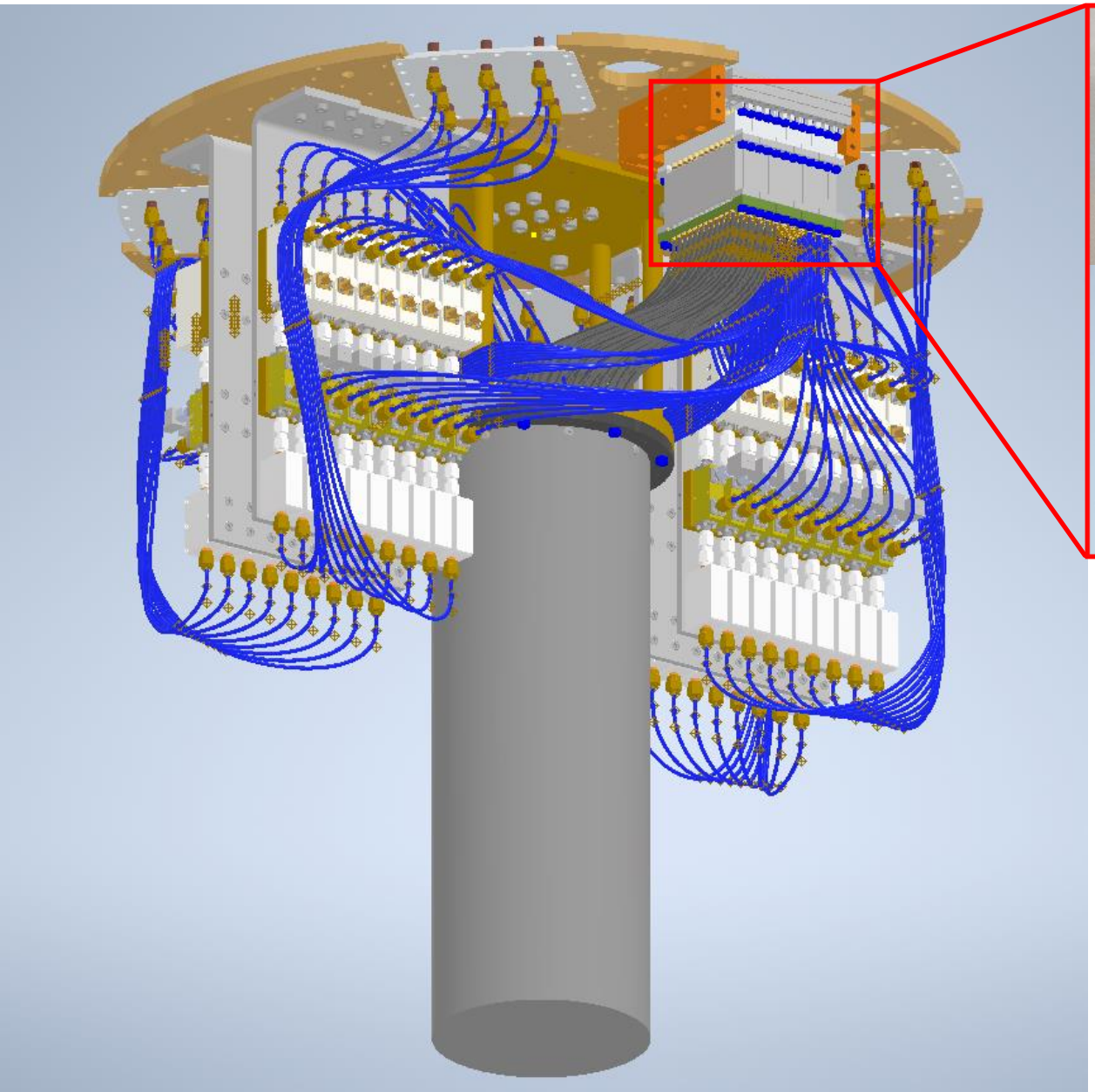
144Q system

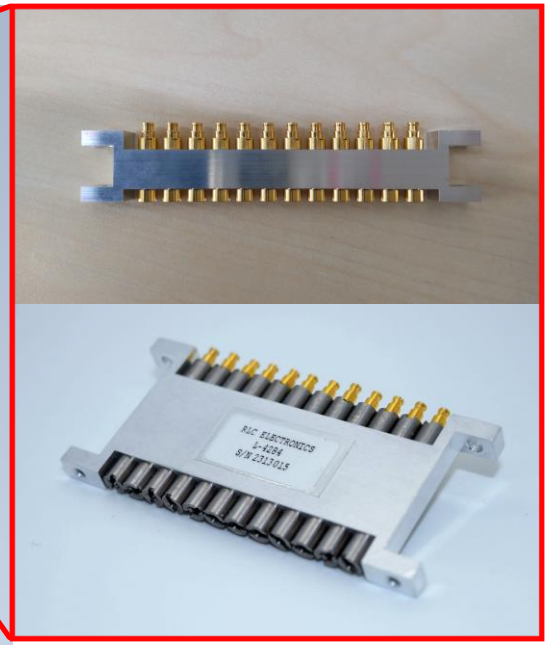


Eccosorb IR filter
Lowpass filter
Highpass filter
Circulator
Isolator
Directional coupler
Terminator



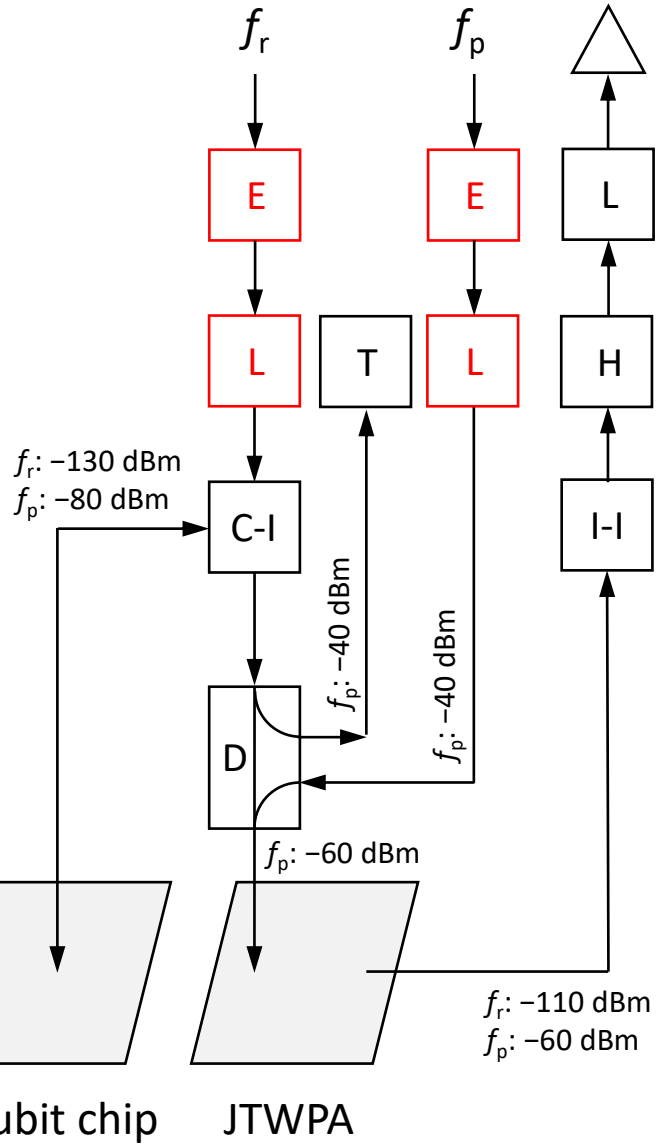
144Q system



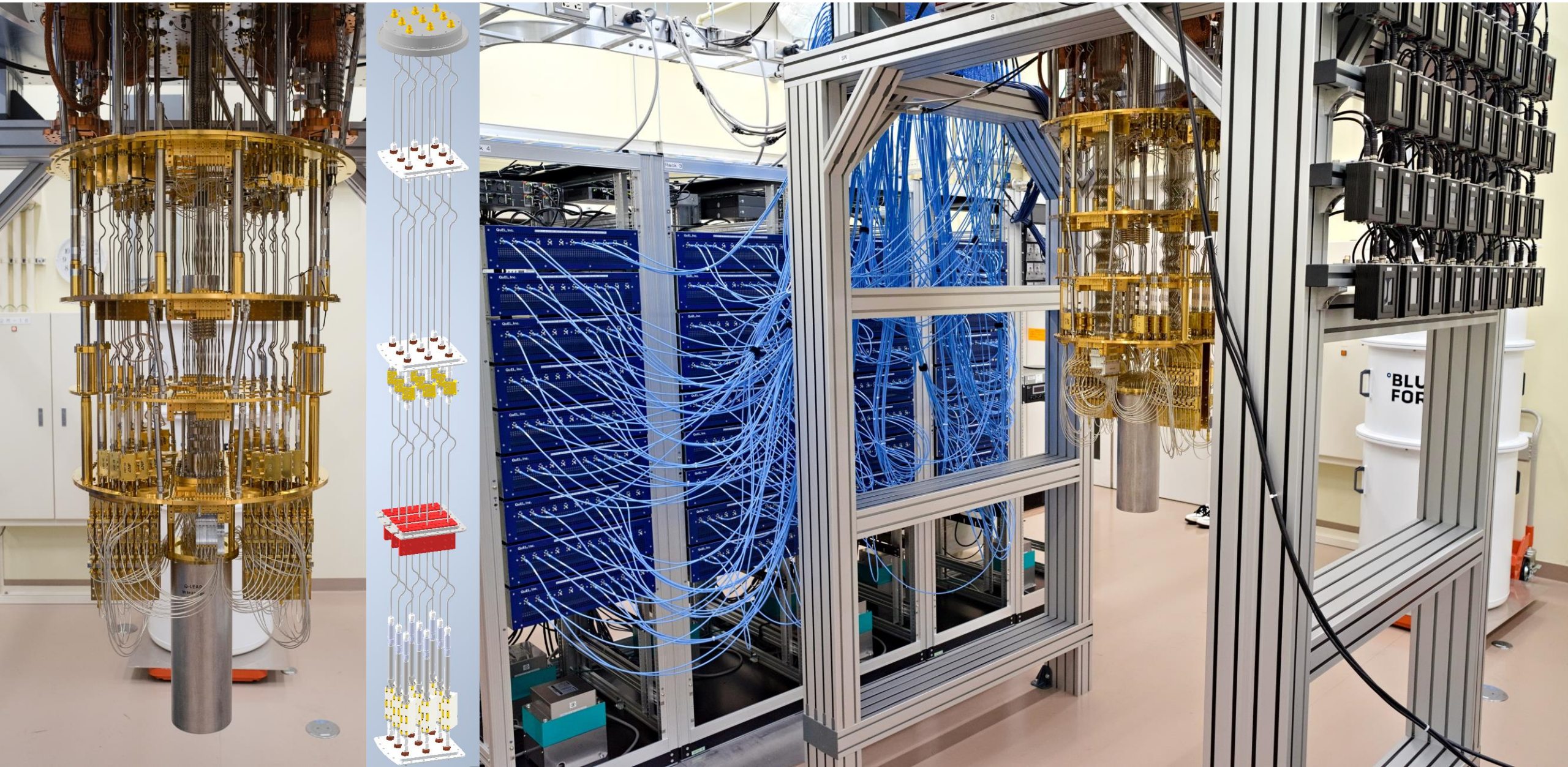


12-way IR & lowpass filters

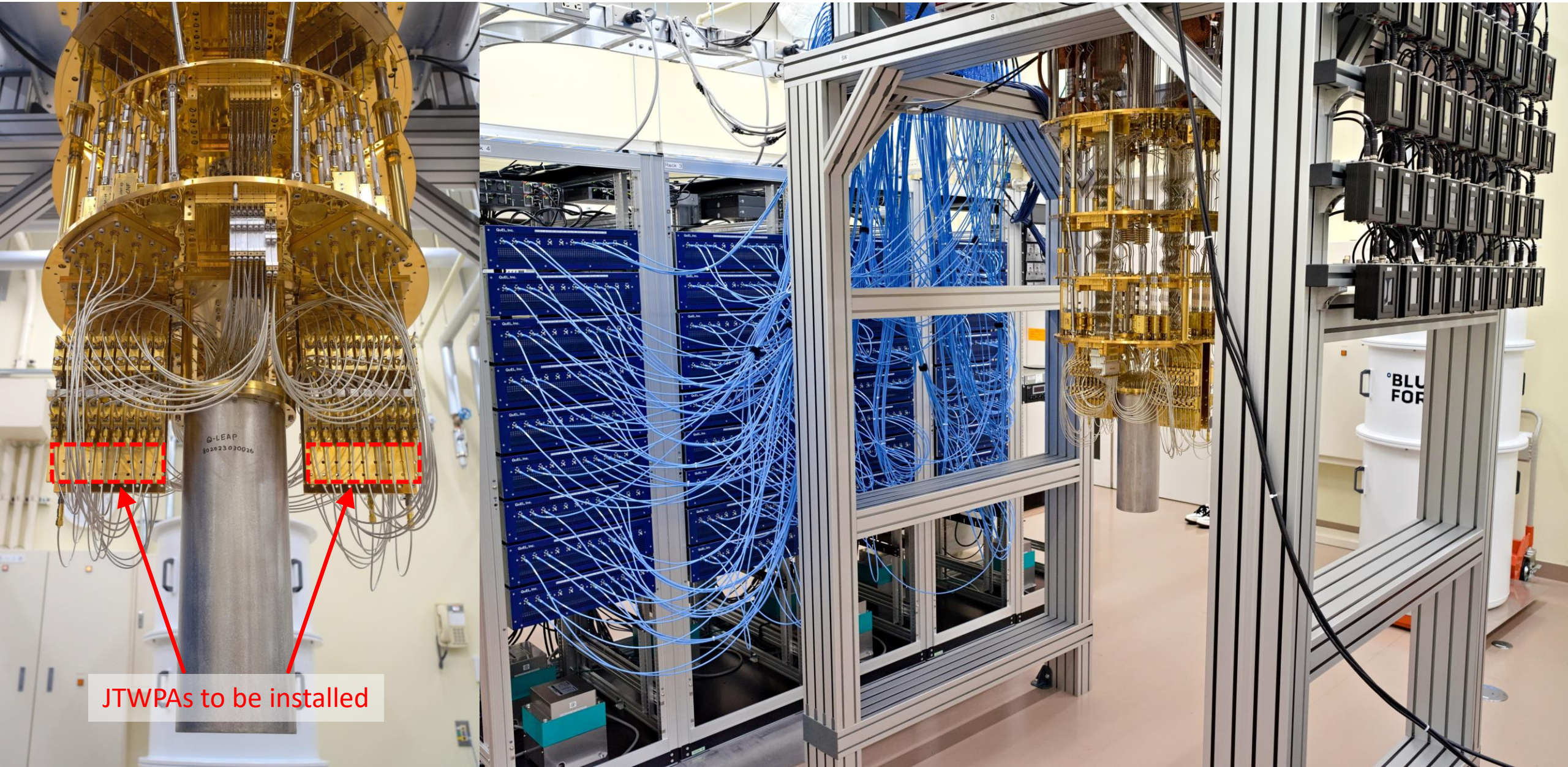
Eccosorb IR filter
Lowpass filter
Highpass filter
Circulator
Isolator
Directional coupler
Terminator



144Q system

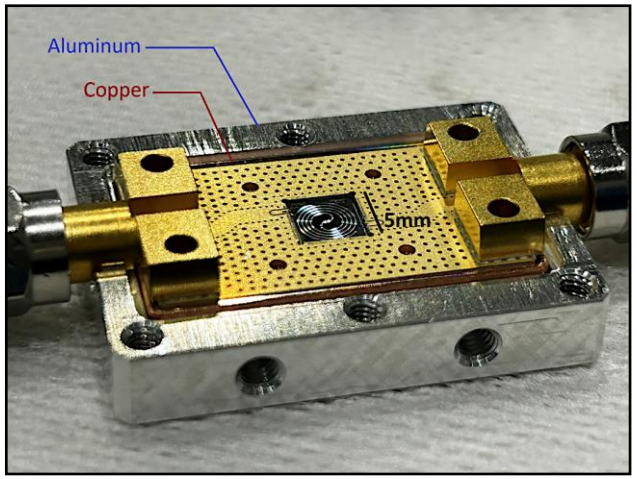


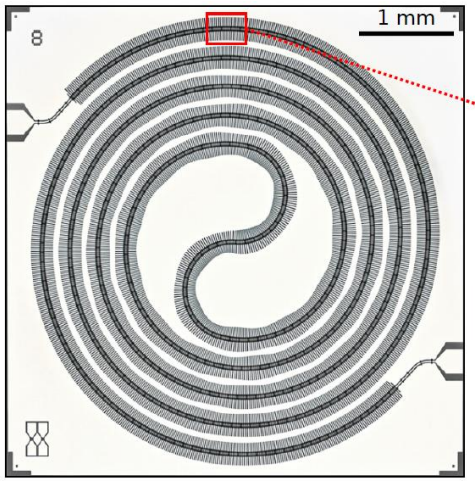
144Q system

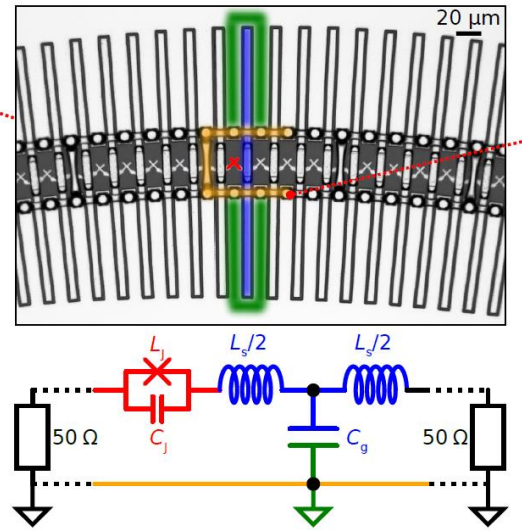


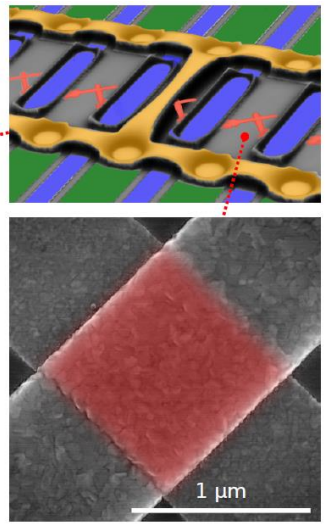
Development of JTWPA

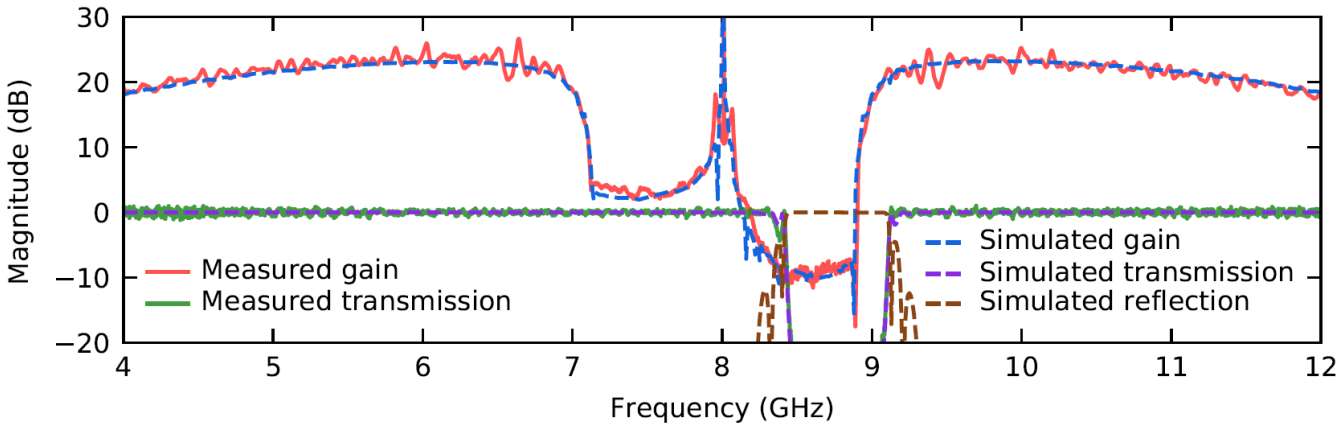
arXiv:2503.07559 **C. W. Sandbo Chang** *et al.*
(New design) MAR-S09: Thu. March 20, 11:54am–12:06pm **C. W. Sandbo Chang** *et al.*
"A waveguide-based resonant-phase-matching JTWPA with efficient phase correction"









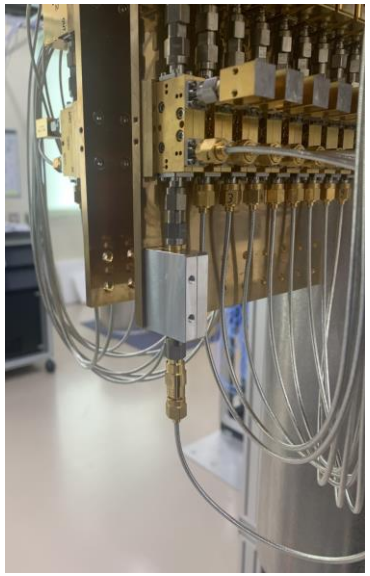


- Open CPW stubs as low-loss shunt capacitors
- 20–23 dB gain over 5 GHz bandwidth
- Gain-ripple suppression by windowed modulation

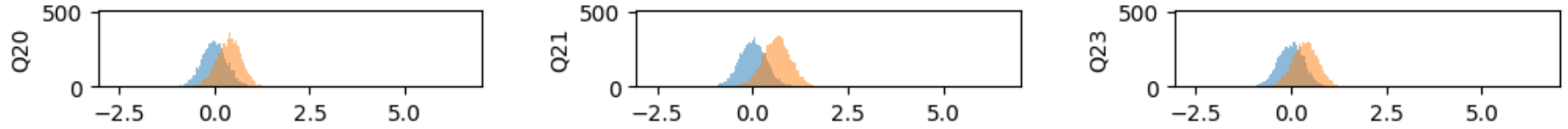
Preliminary characterization of a 144Q system

Characterized by **Shuhei Tamate, Shiyu Wang**

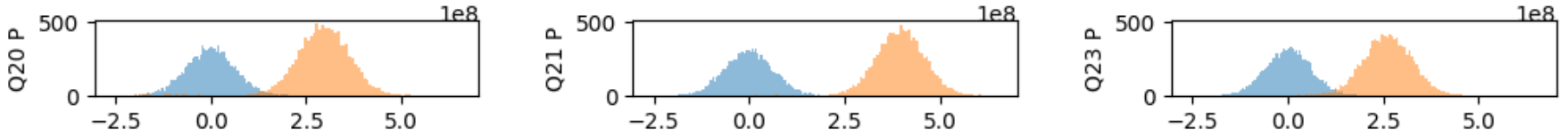
- 105/144 qubits measured
- **Longest relaxation times from a 144Q chip: T_1 = 154 µs, T_{2e} = 272 µs (@5 GHz)**
- Challenge: Better flip-chip bonding of larger chips



Qubit readout **without** JTWPA



Qubit readout **with** JTWPA



Summary

- **64Q hardware**
  - Developed(-ing) technologies for **tileable qubit architecture**
  - Best fidelities exceed 99%, but **plenty of room *for improvement* at the bottom** (i.e., chip)
- **Future works**
  - Test of a 144Q system
  - Run (primitive) algorithms/error correction with larger quantum circuits